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THE DELTIC CORRELATOR

BY
VICTOR C. ANDERSON

JANUARY 5, 1956

ACOUSTICS RESEARCH LABORATORY
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Abstract

The design of a Deltic correlator, a time compression correlator which generates correlation functions on a real time base, is described. The correlator is designed to operate primarily with random noise signals in the audio spectrum (100 c/s to 10 kc/s) and display the first 10 ms of the cross-correlation function of two input signals.

A discussion of the principles of operation of such a device is followed by the consideration of various problems associated with the circuit design, and with a description of alignment and servicing procedures used in the operation of the Deltic. The experimental performance results show the correlator to follow closely the theoretical predictions of signal-to-noise ratio enhancement for weak signals in a thermal noise background. An attempt has been made to explain the minor discrepancies on an empirical basis.

Acoustics Research Laboratory

Division of Engineering and Applied Physics

Harvard University, Cambridge, Massachusetts

Preface

The project of construction of the Deltic correlator described in this report was undertaken by the author while on a one-year post-doctoral research fellowship at the Acoustics Research Laboratory. The correlator was in operation in May of 1955, eight months after the beginning of the project.

The initiation of the project was due primarily to the interest and guidance of Professor F. V. Hunt, for which the author is deeply indebted. Thanks are due also to W. P. Raney for detailed criticism of the manuscript, proofreading, and aid in preparation of the illustrations. In addition to the helpful assistance of the other members of the Acoustics Research Laboratory staff, the author would like to acknowledge the valuable technical assistance in circuit design rendered by members of the Acoustics Branch of the Naval Ordnance Laboratory, Silver Spring, Maryland.

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THE DELTIC CORRELATION

by

Victor C. Anderson

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Chapter I

PREAMBLE

The term Deltic (an abbreviation for Delay line Time Compressor)* is applied to a time compression scheme which makes it possible to apply continuously, without loss of any information, signal "processing" methods such as spectrum analysis, and cross- or auto-correlation analysis to enhance the signal-to-noise ratio of an incoming signal. Time compression in the Deltic is accomplished by sampling a portion of an incoming low-frequency signal, of duration T', at N different times separated by the shorter interval, or "sampling" period T. The sequence of N nearly instantaneous samples obtained in this manner is then squeezed together to form a high-speed replica of the incoming signal--a replica having a smaller total duration just equal to T, the interval between samples. The information of the original signal is now contained on a compressed time scale in this high-speed replica where the time compression factor is given by T'/T, which is equal to N, the number of samples. This replica is then stored in a high-speed recirculation storage channel of recirculation period T so that the compressed information is readily and repetitively available for the convenient application of signal processing methods.

In practice, this time compression and sampling process is carried out in a continuous manner by removing the oldest sample in the replica and replacing it with a new one each time the replica completes another cycle of

*This analysis technique was first described in the University of California Marine Physical Laboratory Quarterly Report for 1 January to 31 March 1954, SIO Ref. 54-18.

circulation in the storage channel. In other words, each sample selected from the incoming low-frequency signal is introduced at the beginning of the replica; it then precesses slowly through the replica until, after an interval T', it will have appeared N times at the output of the storage channe' in the course of progressing from the beginning to the end of the sequence of samples, after which it is removed.

In the typical signal processing methods mentioned above, the incoming signal is usually to be multiplied by some comparison signal and the product then averaged over a short but finite length of time. Ordinarily this multiplying and averaging process must be carried out many times on the same signal while varying some parameter of the comparison signal, such as the frequency, in the case of spectrum analysis, or the relative time delay, in the case of correlation analysis. By using the time compression properties of the Deltic, processing operations which would involve averaging times of T' on the original signal can be carried out equally well on the high-speed replica with the much shorter averaging time T. In this way, N multiplying and averaging operations may be carried out within the duration of the original signal T'. This factor of N is exactly that required to extract all of the information in a signal of length T' during a time interval T' by the above signal processing methods.

As a result of the time compression of the high-speed replica, all of the frequencies in the spectrum of the original signal are multiplied by a factor N. If a spectrum analysis of the incoming signal is desired, it may be obtained by feeding the replica to a conventional sweep-spectrum analyzer covering the multiplied high-frequency band. The analyzer operating in this high-frequency region will have a wider filter bandwidth with a correspondingly shorter response time. Thus a spectrum resolution which would require a filter having a response time of T' if operating on the original signal, may be obtained with a filter having the much shorter response time T operating on the compressed replica. Because of the shorter filter response time, the spectrum level may be determined for N separate frequencies in the band during the time that would have been required to obtain the spectrum level at a single frequency by operating on the original signal without benefit of a Deltic.

The short-term auto-correlation function of a signal is obtained by multiplying a sample of incoming signal of length T' by a corresponding sample which has been delayed slightly. The instantaneous product is averaged over the length of the sample T', and this process of multiplication and averaging is then repeated for a succession of different relative delay times. The output of the multiplier-averager plotted against the relative delay time is the correlation function desired. In the Deltic, the relative time delay is achieved by making use of the precession of data samples through the high-speed replica as described previously. A second storage channel is used to provide a "stationary" reference or comparison signal which consists of the sample sequence in the replica at an arbitrary time t_o. This "stationary" replica is then multiplied by the precessing replica in the Deltic and averaged over the recirculation period T. In each successive recirculation period, the relative delay between the "stationary" replica and the precessing replica increases by one sampling interval; thus, at the end of a time interval equal to the length of the original low-frequency signal (now represented by its time-compressed replica), the average product will have been obtained for N different values of delay. These N delay values correspond to a total time delay for the correlation function of T' which is just equal to the length of the original signal. After the period T', a new replica can be placed in the "stationary" storage channel, and a new short-term correlation function can then be obtained during the next time interval T'. In this way, none of the information in the incoming signal will be lost since there will be no gaps between successive segments of the signal which are "processed" one after the other.

The cross-correlation of two independent input signals can be obtained by using a Deltic for each input to obtain a high-speed replica of each signal. The replica of one of the input signals may then be stored in the "stationary" storage channel, and compared with the precessing replica of the other input signal.

It would appear from the foregoing that the averaging time of such a Deltic correlator would be limited to the length of the original signal, T'. As far as the Deltic correlator itself goes, this is true; but the averaging time can be extended by superimposing a number of the correlation curves

so obtained to form a composite average. Additional time averaging of this kind would ordinarily be incorporated into any practical correlation "processing" system in order to obtain further signal-to-noise-ratio enhancement. Such an additional time-averaging process has been accomplished in the Deltic correlator by the use of a dielectric recorder in which the average of a large number of correlation sweeps is built up as an electrostatic surface charge pattern on a rotating dielectric-coated drum. By the use of this technique, the effective averaging time, which is an important factor in the signal-to-noise enhancement of any such processing system, may be increased almost without limit.

The feasibility of the system which has been described has been demonstrated by the construction and successful operation of the complete Deltic cross-correlator shown in Fig. 1. This Deltic has a time compression factor N, of 300, and stores 10 ms of any incoming low-frequency signals lying within the frequency band extending from 100 c/s to 10 kc/s. The averaging time has been extended from the basic 10 ms of the Deltic correlator itself to a time which may be varied between 0.1 second and 100 seconds by the addition of a dielectric recorder at the correlator output.

Extensive signal-to-noise measurements on the Harvard Deltic have shown agreement, within 0.8 db, with the theoretical predictions of signal-to-noise ratio for a "clipper correlator," for integration times ranging from the basic 10 ms to a drum integration time of 1 second. The effect of this noise reduction is shown in Figs. 2a, b, c. Figure 2a shows an input signal which is composed of two parts: an incoherent noise consisting of an octave band of thermal noise 1600 to 3200 c/s, and a statistically independent "signal" 25 db lower in power having the same spectrum. Figure 2b, which shows the output of the correlator before further integration by the dielectric recorder, is obtained when the noise-plus-signal of Fig. 2a is introduced in one input of the Deltic, and is cross-correlated with a delayed replica of the signal alone supplied to the other input. Figure 2c illustrates the manner in which the longer averaging time made available by dielectric drum integration serves to reduce still further the background fluctuation. Thus, the cross-correlation function of the low-level signal buried in the noise trace of Fig. 2a is now readily detected in the center of the 10 ms sweep shown in Fig. 2c.

Figure 3 shows a similar test in which the "signal" is a sine wave 25 db lower than the noise.

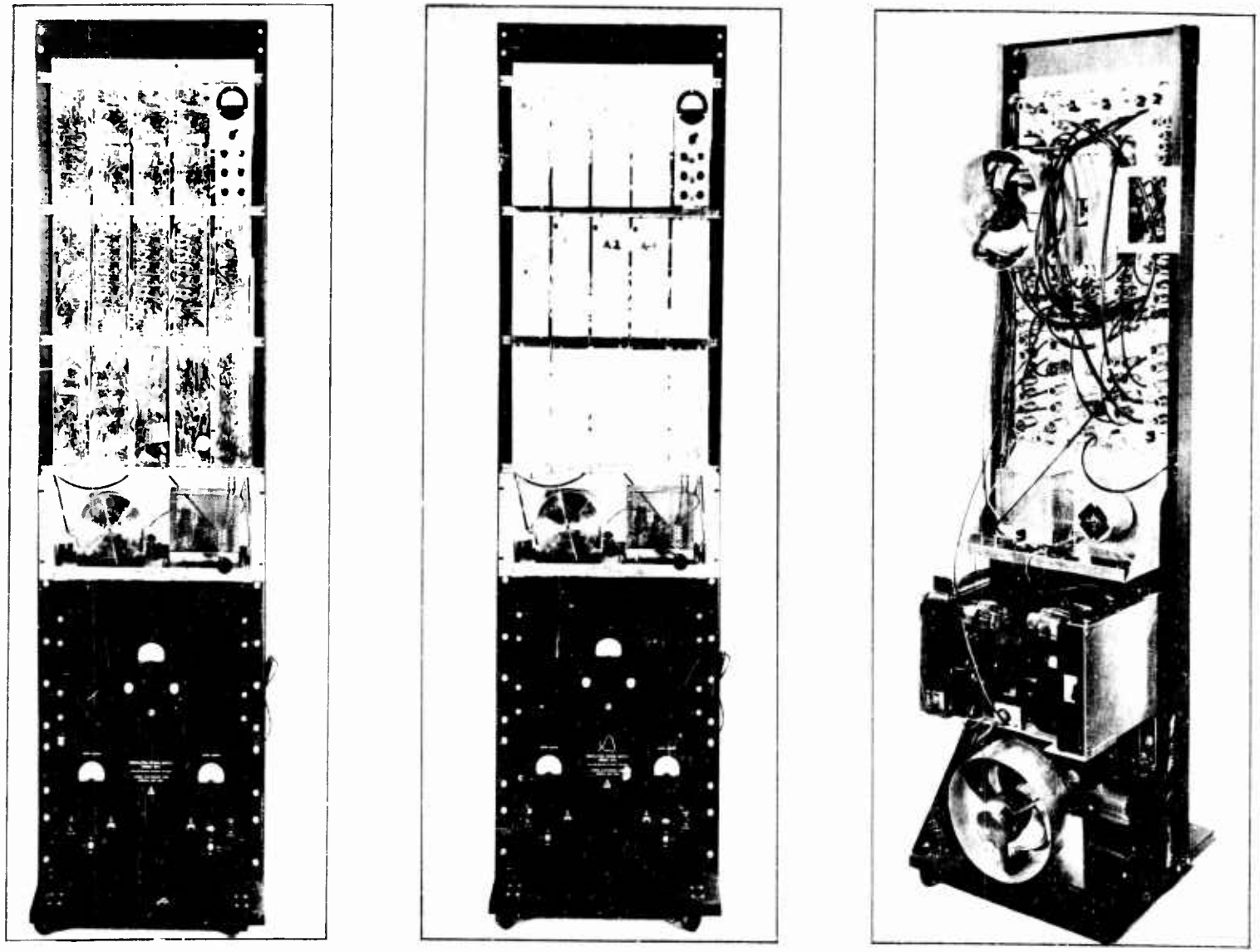


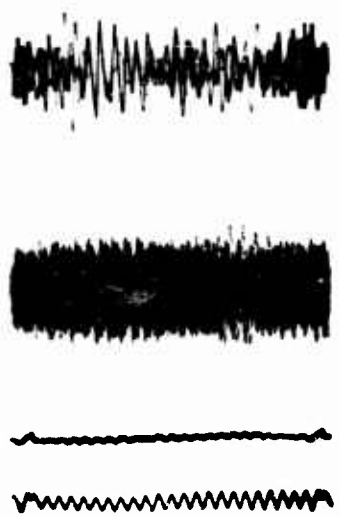
Fig. 1. Harvard experimental Deltic correlator.

2a. INPUT (OCTAVE BAND NOISE & SIGNAL)

2b. CORRELATOR OUTPUT BEFORE INTEGRATION

2c. OUTPUT OF DIELECTRIC RECORDER

Fig. 2. Signal-to-noise measurements (octave band).



3a. INPUT (OCTAVE BAND NOISE & SINUSOIDAL SIGNAL)

3b. CORRELATOR OUTPUT BEFORE INTEGRATION

3c. DIELECTRIC RECORDER OUTPUT (SIGNAL OFF)

3d. (SIGNAL ON)

Fig. 3. Signal-to-noise measurements (sine wave).

Chapter II

PRINCIPLES OF OPERATION OF A DELTIC CORRELATOR

A. Definition of "Correlation Function"

The general correlation function is given by:

$$\rho_{xy}(\delta) = \lim_{T\to\infty} \frac{1}{T} \int_0^T x(t)y(t-\delta)dt, \qquad (1)$$

where x(t) is a time-varying function and y(t) is another time-varying function. The general correlation function of two random signals can never be exactly determined experimentally since both an infinite integration time and a continuum of values of δ are called for. In practice, only finite integration times are employed for analysis, and $\rho(\delta)$ is usually evaluated only for discrete values of δ. The approximate correlation functions obtained in this manner are called short-time correlation functions and are characterized by a certain amount of residual statistical fluctuation comprising "noise" or uncertainty in the resulting function. The properties and applications of such short-time correlation functions have been discussed by several authors, among them R. M. Fano [1], and Faran and Hills [2].

The correlation functions generated by the Deltic are further approximations to the short time correlation functions. The sampling process of the Deltic quantizes the incoming x and y signals into pulse trains composed of discrete polarity samples; that is, each signal is represented by a train of "sample" pulses which are of unit height when the signal is positive, and of zero height when the signal is negative. The product of these pulse trains is averaged over the length of the stored sample to generate the points on the correlation curve. The nature of the approximate correlation functions generated by the Deltic is shown by the equation:

$$\rho_{xy}(mT) = \frac{1}{N} \sum_{n=0}^{N} \hat{x}(n\tau)\ \hat{y}(n\tau - m\tau), \qquad (2)$$

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(1) R. M. Fano, "Short-Time Autocorrelation Functions and Power Spectra," J. Acoust. Soc. Am. 22, 546-550 (December 1950)

(2) J. Faran and R. Hills, T.M. 27, Harvard University Acoustics Research Laboratory.

where N represents the number of samples in the stored pulse train, T is the period at which the low-frequency signal is sampled, τ is the pulse repetition period in the time-compressed replica, and the functions $\hat{x}$ and $\hat{y}$ are the clipped, time-compressed replicas of the original functions. The quantities m, n and N are all integers, and m takes on values between 0 and M. It can be shown that the effective integration time is equal to the sample length NT. In operation, this summation is carried on in a progressive manner, m changing by one integer each time that n runs through the range 0 to N. Thus it can be seen that the correlation function $\rho_{xy}(mT)$ is generated on the same time base as the original signal. If M = N, the correlator sweep range, which is equal to the time spent in the analysis, will also be equal to the length of the stored signal, and the analysis will be performed with no loss of incoming information. The index n corresponds to the position of a digit in the pulse train while m is the position index of a pulse train in the correlation sweep.

The effective integration time of the summation indicated in Eq. (2) is equal to the original length of the low-frequency signal which is time-compressed and then stored in the recirculating pulse train. This effective integration time is determined by the length of the delay line and the clock pulse period; it is independent of the time duration of the correlation sweep as determined by the period of the transfer pulse, although the two times are usually made approximately equal so as to obtain 100 per cent signal processing. It would be possible, however, to extend the effective integration time of the Deltic correlator output by summing over a number K of consecutive correlation sweeps. In this case, the integration or summation of Eq. (2) is extended to a series of summations as follows:

$$\left\langle \rho_{xy}(mT) \right\rangle_{KM} = \frac{1}{KN} \sum_{k=0}^{K} \sum_{n=kM}^{kM+N} \hat{x}(n\tau)\hat{y}(n\tau - m\tau) \qquad (3)$$

This type of integration, "finite time" integration, is not easy to achieve with electronic circuits. In its place, the averaging properties of an electrical low-pass filter are used where it is necessary to extend the integration time. A dielectric recorder having integrating properties analogous to a simple RC low-pass filter is used in the Deltic to extend the integration by superimposing

successive sweeps with an exponential weighting factor to obtain a running time average. This type of averaging actually amounts to an infinite summation in which the normalized correlation function has the form:

$$\langle \rho_{xy}(mT) \rangle_{T_3} = \frac{1-e^{\frac{-MT}{T_3}}}{N} \sum_{k=0}^{\infty} e^{\frac{-kMT}{T_3}} \sum_{n=kM}^{kM+N} \hat{x}(n\tau)\hat{y}(n\tau - m\tau) \tag{4}$$

Faran and Hills point out that the effective integration time of an RC averaging network of this type (as determined by its effectiveness in reducing short-term correlation noise) is equal to twice the time constant. Thus the equivalent number of correlation sweeps contributing to the average output of the dielectric drum is equal to the number of sweeps occurring in a period of $2T_3$, where T_3 is the build-up time constant of the drum. The total effective integration time of the Deltic including the dielectric recorder will be the product of the stored signal length and the number of sweeps contributing to the average; i.e.,

$$T_2 = NT \times \frac{2T_3}{MT} = \frac{2N}{M} T_3$$

B. Deltic Parameters

The basic parameters of the Deltic, some of which were introduced above, are related by simple equations defining the operating limits of this technique. These parameters may be summarized as follows:

- T = the sampling pulse period, pulse train length, or delay line recirculation period.
- τ = the clock pulse period or the digit separation in the pulse train.
- N = the number of digits in the pulse train.
- f_o = maximum allowable frequency of incoming signal as determined by Shannon's sampling theorem.
- T' = the length of the low-frequency signal represented by all the information in the pulse train.
- M = the number of sample pulse periods in the correlation sweep.
- T_1 = the correlation sweep range.

T_2 = effective post-detection integration time.

T_3 = dielectric recorder time constant.

These are related in the following manner:

$$N = T/\tau; \quad (5)$$

$$N = T'/T; \quad (6)$$

$$f_o = 1/2T; \quad (7)$$

$T_1 = MT$

T_2 = T' without dielectric recorder post-detection integration; with dielectric integration, and when $T_3 >> T'$:

$T_2 = \frac{2NT_3}{M}$ for $M > N$;

$T_2 = 2T_3$ for $M < N$.

The three independent relations (5), (6) and (7) fix the number of independent parameters at two out of the first five listed. Regardless of which two parameters are used as design criteria, the Deltic characteristics are ultimately determined by the selection of values of T and τ. Both T_1 and T_2 may be varied independently by a suitable choice of M and recorder time constant respectively.

The accompanying table (Table I) lists some typical Deltic characteristics which can be obtained by different choices of the recirculating pulse repetition time τ (here chosen to be 0.1 μsec) and of the length of delay line T.

C. Computing Logic of a Deltic Correlator

A clearer conception of the significance of the Deltic parameters may be had by following in detail the various computing operations of a Deltic correlator through a complete computing cycle. The computation may be considered in two parts: first, the basic time-compression sampling process which takes place in the sampling channel; second, the process of obtaining a correlation function from this time-compressed information.

It was mentioned in Chapter I that the heart of the Deltic consists of a recirculation delay-line storage channel or memory. This type of memory is well known in computer work. The information is stored as a wave packet or pulse in a closed transmission loop which consists of an acoustic delay path with appropriate electrical transducers, an amplifier and a reshaping

Table 1

TABLE OF TYPICAL DELTIC CHARACTERISTICS

Delay line length required, T	30 μsec	100 μsec	300 μsec	1000 μsec	3000 μsec
Pulse separation in line, τ	.1 μsec	.1 μsec	.1 μsec.	.1 μsec	.1 μsec
Length of stored record	.009sec	.1 sec	.9 sec	10 sec	90 sec
Length of correlation sweep for 100% processing	009 sec	.1 sec	.9 sec	10 sec	90 sec
Max. frequency of input signal	16.5 kc/s	5 kc/s	1.65kc	500 c/s	165 c/s
Correlation delay resolution	30 μsec	100 μsec	300 μsec	1000 μsec	3000 μsec
Max. frequency resolution	110 c/s	100 c/s	1.1c/s	.1 c/s	.011 c/s
Time compression factor or the number of analysis points per sweep	300:1	1000:1	3000:1	10,000:1	30,000:1

circuit. Provision for introducing or removing individual pulses is made by the use of suitable electrical gate circuits.

An illustration of the sampling process which converts such a recirculating memory into a Deltic is shown in Fig. 4. The original low-frequency signal is shown in the upper part of the figure by the undulating line. The vertical lines shown with the separation of T represent the times at which a sampling pulse will introduce the new information into the re-circulating memory which has a recirculation time $T-\tau$. The sequence of pulses at the output of the delay line is shown in the center of the figure where the pulses are represented by the short vertical lines appearing above the base line. The expanded view at the bottom of the figure represents the actual form of the envelope of the signal at the output of the delay line for 1 repetition

period T. Since the storage is binary in nature, only the polarity of the low-frequency signal is introduced as information into the line. This is an extreme case of quantitization in amplitude, but for random signals it does not give rise to an objectionable loss of signal-to-noise-ratio information. The operation of the sampling process may be understood by following the sequence of sampling pulses and their associated data pulses in the line. At sample point (a), the positive polarity of the low-frequency signal is introduced as a pulse into the delay line. At the end of the recirculation period $T-\tau$ this pulse appears at the end of the delay line as shown by digit (a) in the center of the figure. One digit later, the sampling pulse introduces a new data sample which again corresponds to a pulse because of the positive polarity of the low-frequency signal at that instant of time, and this pulse is circulated through the line, appearing on the output after a period $T-\tau$. In the meantime, the digit (a) has been re-entered into the line and has appeared at the output just ahead of digit (b), or two digit spaces before the sampling pulse. The process continues as illustrated in the figure. When the polarity of the incoming low-frequency signals is negative, the information is conveyed by the absence of a pulse as illustrated by digit (d) in the output of the delay line. After the line is completely full, the sampling pulse operates, not only to introduce new information into the line, but also to erase the data pulse which normally would be advanced to the sampling pulse position.

In view of the N-fold redundancy present in the output of the delay line as evidenced by the fact that a single data sample appears in the output N times, where N is the number of pulses in a pulse train of duration T, one may look at the high-frequency replica of the low-frequency signal N times during the storage period of a single data sample. This is the property of the Deltic which makes it possible to perform the signal processing techniques mentioned in Chapter I in a serial rather than parallel manner.

This sampling process has a special property which makes the Deltic ideally suited for the computation of correlation functions. This property is illustrated in Fig. 4 where it can be seen that a single data sample in the pulse train advances by 1 digit position each sampling interval. This relative time advance of the high-frequency replica of the low-frequency signal is used

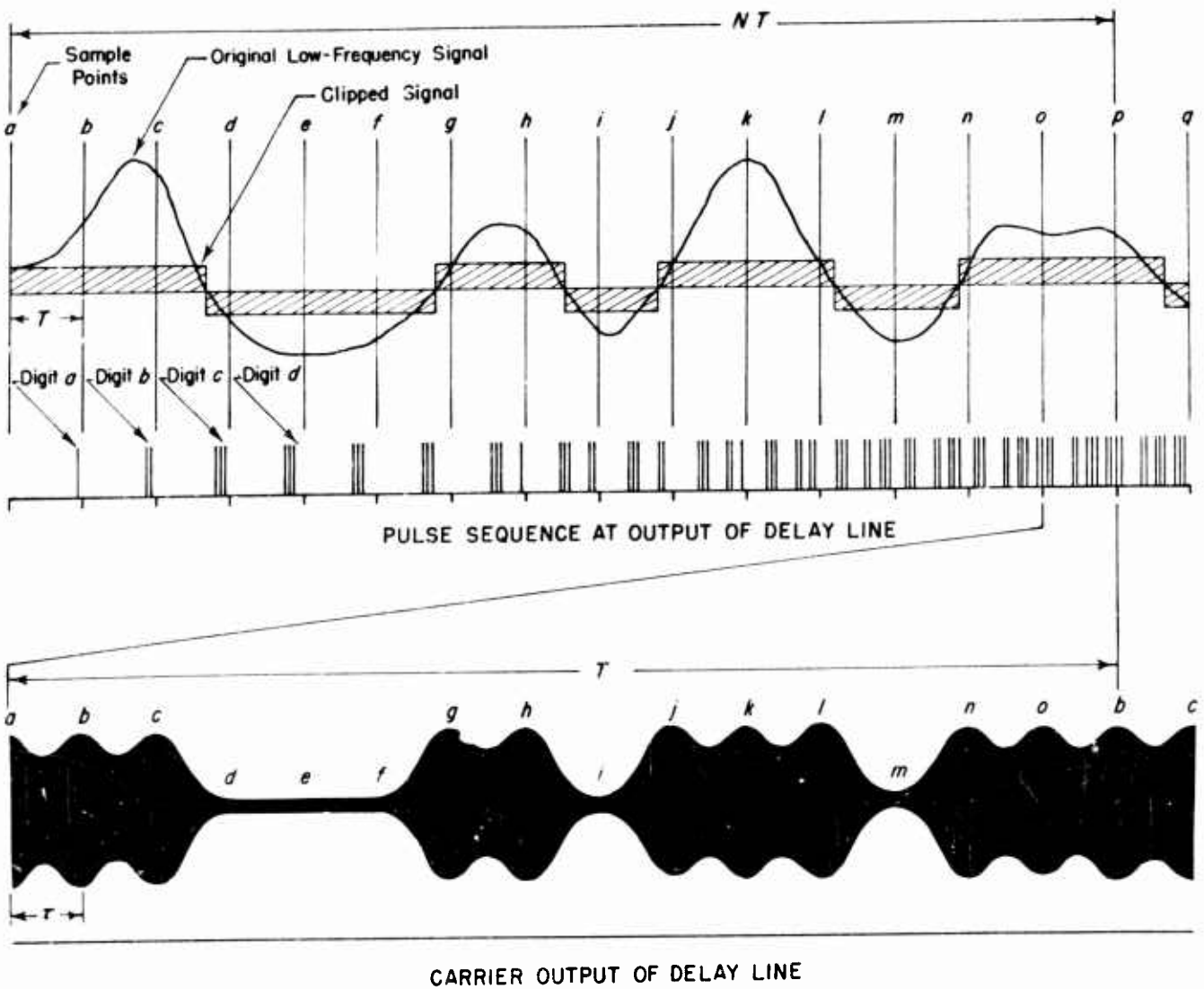


Fig. 4. Illustration of the Deltic sampling process.

to provide the necessary incremental time delay when generating auto-correlation and cross-correlation functions.

In order to make use of the relative time advance of information introduced by the sampling process, an auxiliary "stationary" storage channel must be provided to retain a comparison pulse train in which there is no progressive advance of information. It should also be noted that each of the pulse trains (i.e., a complete time sequence of samples) as illustrated at the bottom of Fig. 4 is 1 digit longer than the basic recirculation time $T-\tau$; therefore, the storage channel must have a recirculation time of T instead of that of the sampling channel, $T-\tau$, so that the beginning and end of a train of information in the two channels will always be in synchronism.

The manner in which correlation functions are generated by a Deltic is illustrated by Fig. 5. Here a representation similar to Fig. 4 is used, but the input is shown to be a periodic square-wave signal rather than the random noise signal of Fig. 4. This square-wave input, of course, corresponds to the clipped sine-wave input, so the correlation function shown is the same as that produced by a sine-wave input to the Deltic correlator and is an approximate correlation function for a square wave. The output of the delay line which is used for sampling the incoming data is shown in line B of the figure. Line C corresponds to the output of the auxiliary storage channel mentioned above. At some arbitrary time interval, illustrated by the interval T at the left of the figure, the pulse sequence from the sampling channel (line B) is transferred to the storage channel (line C) and is repeated periodically in this channel as shown by the recurrence of this particular pulse sequence in each of the successive sampling-time intervals. The value of the correlation function for zero-delay time is obtained by measuring the coincidences of pulses in the sampling channel and in the storage channel during this first time interval T. This coincidence output is represented by line D of the figure, where the presence of a pulse represents a coincidence, and the absence of a pulse represents an anti-coincidence between the two channels. The zero-delay time, or the first time interval, gives complete coincidence for all pulses and corresponds to a correlation of +1. In the next time interval T, the two pulse trains have

been displaced by one pulse period, and we see that now there are several anti-coincidences appearing in the lower pulse sequence. This results in a lower value of correlation and is shown by the step of the staircase trace E, which represents the correlation output. Continuing on, we see that each successive time interval yields a lower number of coincidences, until, in the fourth interval, we get a complete anti-coincidence for all pulses. This gives a value of -1 in the correlation function. From this point, the pulse trains in the sampling channel and in the storage channel again approach a phase error of zero and the correlation function rises in a stepwise manner to the value of +1 again. This broken curve, E, is the type of output obtained from the Deltic correlator and corresponds to the actual correlation function of the square wave illustrated by curve F superimposed upon the broken curve. The length of the correlation sweep T_1 shown at the bottom of the figure was deliberately chosen to be longer than the length of the stored signal T' shown at the top of the figure in order to emphasize the fact that the correlation sweep time for correlation sweep length is independent of the stored record and need only be equal to it when 100 per cent signal processing is desired. At the end of the correlation sweep T_1, the information in the storage channel is replaced with a new pulse train from the sampling channel and the generation of the correlation function is repeated.

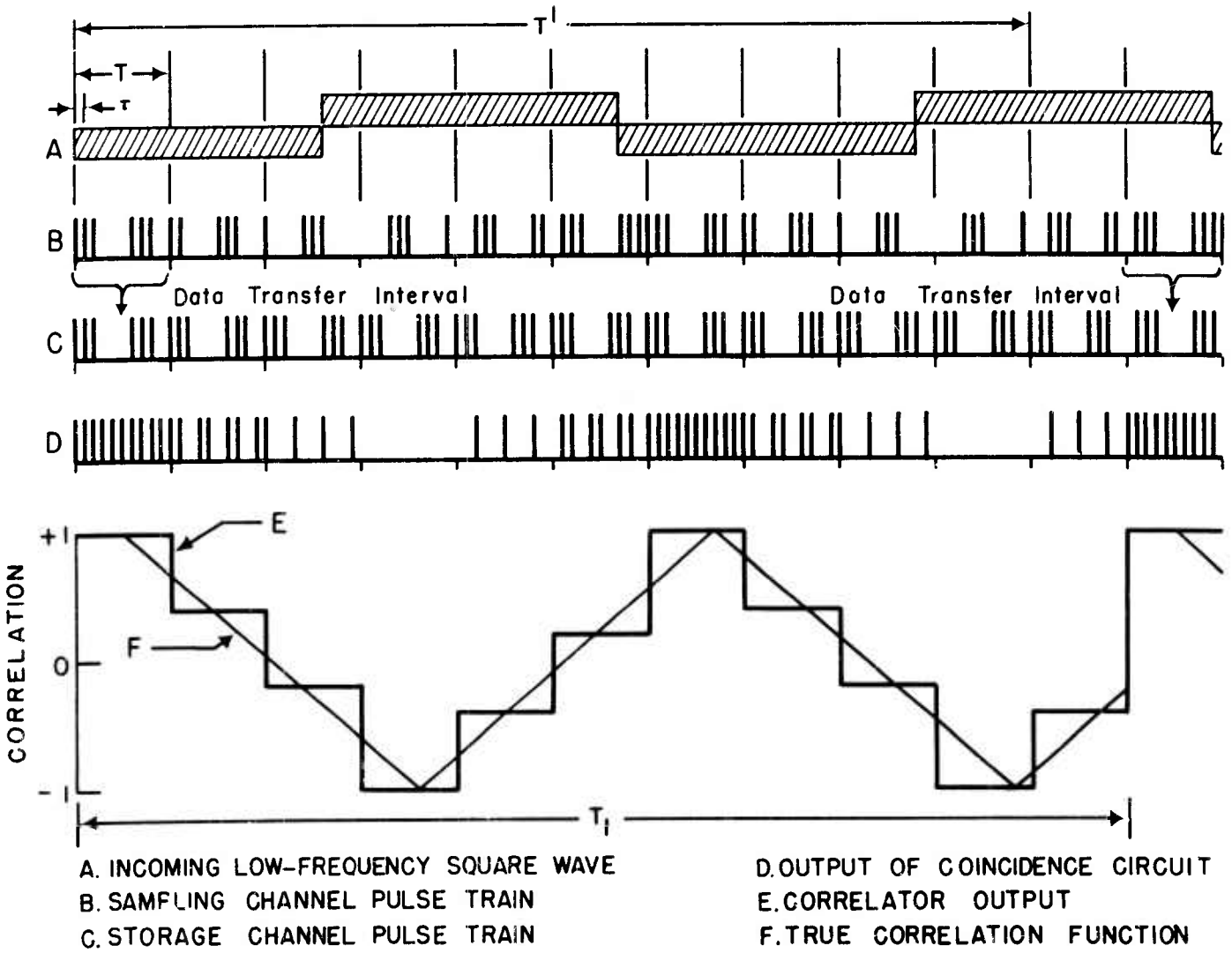


Fig. 5. Illustration of the generation of a correlation function with the Deltic correlator.

Chapter III

DEVELOPMENT OF DELTIC CIRCUITRY

In this chapter, the major design considerations which arose during the development of the experimental Deltic correlator at Harvard will be set forth. For want of a better criterion, they will be discussed in the chronological order in which the various problems were attacked.

The parameters for this experimental correlator were chosen more or less arbitrarily, so that the instrument would have a high-frequencey cut-off of 15 kc/s, covering the audio spectrum, and would operate with a clock pulse period of 0.1 μsec, this being considered a realistic minimum period for the present state of the art. The choice of these two parameters, and Eqs. (5), (6) and (7), fixed the following design constants:

$$
\begin{aligned}
T &= 30.7\ \mu\text{sec}\ (30\ \mu\text{sec quartz delay line} \\
&\quad +0.7\ \mu\text{sec amplifier and cable delay}), \\
\tau &= 0.1\ \mu\text{sec}, \\
N &= 307, \\
f_o &= 16.3\ \text{kc/s}, \\
T' &= 9.42\ \text{ms}.
\end{aligned}
$$

The length of the correlator sweep was chosen as close as convenient to the length of stored signal so that the information processing would be nearly 100 per cent effective. M was fixed by a 320:1 scaler used as a frequency divider. This gave a value for T_1 of

$$T_1 = 9.82\ \text{ms}.$$

Since $M \simeq N$, the effective integration time may be considered equal to twice the time constant of the dielectric recorder which may be adjusted over a range of 0.1 to 100 seconds.

As a prelude to the initial design of the Deltic recirculating memory, a frequency-scaled model of the circuit logic was constructed around a 25 ms delay line composed of low-pass filter networks (Burnell Company). The center frequency of the line and the bandwidth of the recirculating amplifiers were scaled to a 3 kc/s center frequency instead of the 30 Mc/s

frequency which was to be used with the ultrasonic delay line. The inter-electrode tube capacities and expected stray wiring capacities were also scaled to this lower-frequency region so that the operation of the gating circuits and pulse amplifiers would more closely approximate the type of operation which was to be expected in the megacycle region. This scale model proved to be very valuable in the initial design inasmuch as several preliminary ideas were rejected and the general gating techniques which proved to be successful in the final model were established on the scale model in short order.

A. General Logic of the Deltic Correlator

The logic used in the final model of the Deltic is illustrated by Fig. 6 where the circuit of an ultrasonic memory as used in the Deltic is shown. The design consideration for the various blocks shown in Fig. 6 will be discussed later in this chapter. The waveforms and amplitudes of the voltages at various parts of the circuit are shown in the figure.

To describe the operation of this circuit, we may consider a pulse arriving at the input to the driver amplifier. The pulse, after passing through the driver amplifier, enters the reclocking gate where it is mixed with the clocking pulse, a very narrow pulse of approximately 0.02 μsec duration and a 10 Mc/s repetition rate. The reclocking gate has a saturation characteristic of such nature that input pulses from the driver amplifier which exceed an amplitude threshold of approximately 20 volts will give an essentially constant impulse to the matching network, while signals which are under 10 volts will give an essentially zero impulse to the matching network. The current pulse out of the reclocking gate is always in phase with the clocking pulse, even when the recirculating pulse has a phase error of as much as $\pm$0.02 μsec. The restoration of the recirculated pulse to a standard amplitude and phase in this manner eliminates the possibility of any cumulative degeneration of the pulses after a number of recirculations in the loop. The current pulse of the reclocking gate rings the matching network and excites the acoustic transducer coupled to the quartz delay line, introducing an acoustic wave packet or pulse which progresses through the quartz to the output transducer. At the output transducer the acoustic pulse is converted back to an electrical signal which has an amplitude approximately

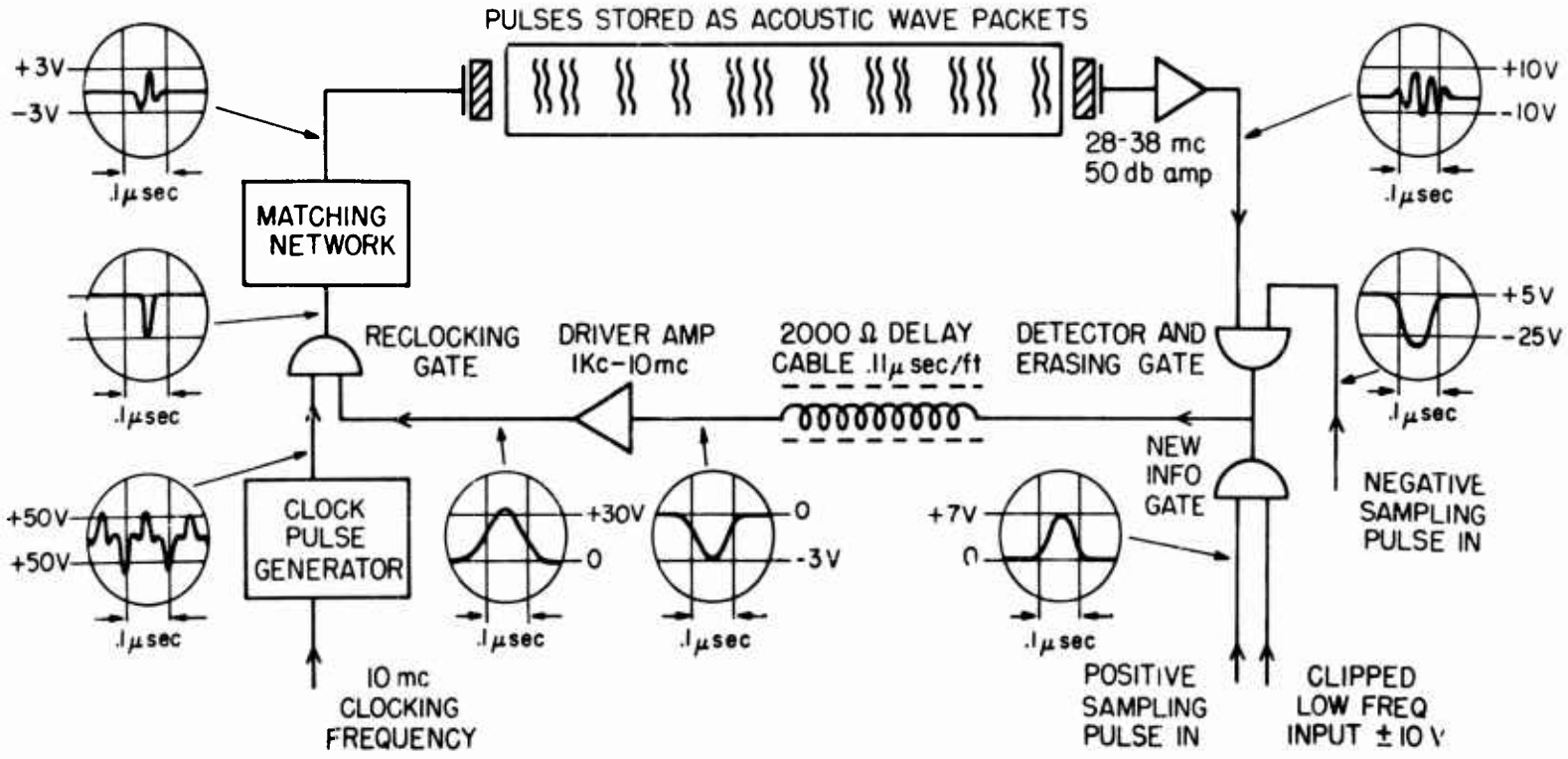


Fig. 6. Block diagram of the recirculating memory used in the Deltic.

50 db lower than the electrical pulse applied to the input. A band-pass amplifier having a gain of approximately 50 db is used to restore the output of the line to a level which will operate the detector.

In the absence of a sampling pulse in either the erasing gate or the new information gate, the detected output of the band-pass amplifier will be transmitted as a pulse through a section of delay cable to the driver amplifier and reintroduced into the delay line as before. The delay cable is used to trim the overall delay path to match an integral multiple of the clock pulse period. It can be seen that once a pulse is introduced into this regenerative loop, it will be recirculated indefinitely in its proper relative position in a pulse train and at a constant amplitude. With the arrival of a sampling pulse, however, the erasing gate will block the passage of the recirculating pulse that arrives at the detector coincidentally with the sampling pulse, while at the same time, the new information gate will simultaneously introduce a new data sample into the recirculating loop. The new data sample will be a pulse if the low-frequency input signal has a positive polarity, or will be "no pulse" if the polarity of the low-frequency input signal is negative.

Two or more recirculating or dynamic memories of this type (more conveniently called channels) are required to form the Deltic. The circuit of Fig. 6 is a sampling channel, used to convert the low-frequency incoming signal to the high-frequency recirculating pulse train. The term Deltic should be applied in the strict sense to this sampling channel, for it is here that the time compression is accomplished.

A channel similar to the sampling channel can be used advantageously to generate the sampling pulse shown as an externally supplied control signal in the right-hand corner of Fig. 6, and to control the 10 Mc/s clock frequency which drives the clock pulse generator. This channel, called the timing channel, is arranged so that one and only one pulse is recirculating at one time. The overall recirculation period or time delay of this channel is extended 1 digit (0.1 μsec) by increasing the length of the delay cable between the detector-and-erasing gate and the driver amplifier so as to generate a sampling pulse of a repetition period T which is 0.1 μsec longer than the recirculation period of the sampling channel of Fig. 6. An automatic

frequency control on the 10 Mc/s clock oscillator locks the phase of the 10 Mc/s signal to the phase of the sampling pulse which is re-circulating in this line. In this way, the clocking oscillator is always locked to a submultiple of the fundamental repetition period of the line, thus providing compensation for temperature changes in the acoustic delay line or in the clock oscillator tank circuit itself.

The various block components of a Deltic correlator are shown in Fig. 7. In addition to the channels previously described, it is necessary to have a storage channel. This storage channel is operated in such a way that one complete pulse train may be transferred to it from a sampling channel and recycled indefinitely. The recirculation period of the storage channel is equal to T so that the start and end of the pulse trains in both a sampling channel and a storage channel will be synchronized. The high-frequency output of the storage channel will be the $\hat{x}(m\tau)$ of Eq. (2), and the output of the sampling channel (a) represents the function $\hat{y}(m\tau - n\tau)$ in Eq. (2). The summation indicated by Eq. (2) is carried out by combining both the output of sampling channel A and the output of the storage channel in a multiplier and averager of averaging period T. The frequency divider shown at the bottom of Fig. 7 generates the transfer pulse which is a pulse of duration T occurring at a repetition period of MT. This transfer pulse is used to transfer the pulse train from sampling channel B into the storage channel. Thus, the correlation function which is the output of the multiplier and averager is recycled at the end of a period MT during which time the correlation delay variable has been swept over a range from 0 to MT.

B. Ultrasonic Delay Lines

The four-channel delay-line package used for the storage lines of the various channels in the Deltic is shown mounted in placed on the relay rack in the right-hand photo of Fig. 1. The complete package has the dimensions of 8" x 4" x 2", and contains four quartz-rod delay lines equipped with piezoelectric transducers at each end. The four rods are clamped in a single brass block which in turn is thermally insulated from the outer case. In this way, the relative temperature difference between the individual lines is kept to a minimum, and

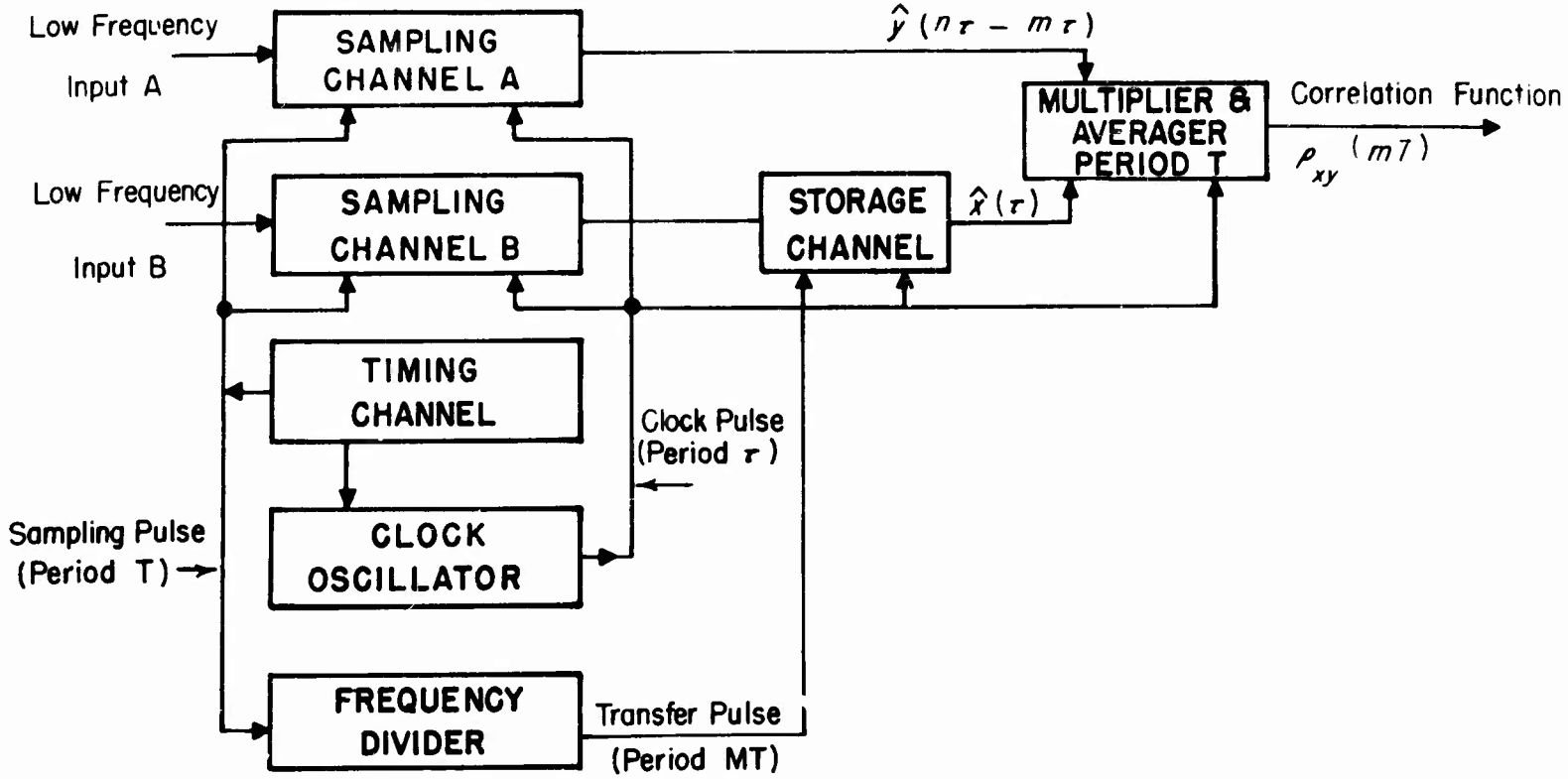


Fig. 7. Block diagram of a complete Deltic correlator.

a regulated temperature enclosure is not required. The delay line package was supplied by Laboratory for Electronics, Inc , of Boston. Each of the lines in the package met the following specifications:

Delay time:	30 μsec matched to within ± 0.01 μ sec
Center Frequency:	30 Mc/s
Bandwidth:	12 Mc/s
"Attenuation":	45 db voltage gain, into a 500Ω termination (with parallel inductor to annul source reactance)
Spurious Response:	-30 db
Transducer Capacity:	30 - 35 μμfd

C. Band-Pass Amplifier

In the design of the band-pass amplifier for the recirculating memories, particular attention had to be paid to the phase linearity of the coupling networks used, as well as to the normal gain and bandwidth requirements. The reason for the relatively high importance of the phase linearity lies in the use of a short broadband pulse for exciting the delay line. When the delay line and amplifier are excited by a short pulse of this type, the shape of the carrier pulse envelope at the output of the amplifier is determined by the transient response of the overall delay line and band-pass amplifier combination. As is always the case for wide-band pulse amplifiers, in order to obtain a well-resolved pulse at the output of the amplifier, the amplifier and delay line combination must have a linear phase characteristic over its useable frequency band in addition to having a sufficiently broad pass band to obtain the desired short rise time.

The selection of an interstage coupling network that would have the desired phase characteristics was based on tests carried out by inserting frequency-scaled models of the coupling network under consideration into the low-frequency recirculation delay-line model as shown in the block diagram of Fig. 8. By adjusting the loop gain to a value slightly less than unity, it was possible to observe the effect of successive stages on the shape of a narrow input pulse. Several coupling networks were checked by this method in order to arrive at a satisfactory circuit. The frequency and phase response of three of these circuits are shown in Fig. 9a, and the corresponding transient responses

shown in Fig. 9b. It can be seen from the waveforms of Fig. 9b that the effects of dispersion after a large number of passages through the coupling network become quite obvious in the case of the overpeaked "L" network. On the other hand, a very well-defined pulse shape is preserved in the linear phase network even after a large number of recirculations corresponding to a large number of coupling stages. The shunt peaked circuit, which is the band-pass equivalent of the conventional shunt peaked low-pass amplifier, was chosen as a coupling network because of its greater simplicity of construction, even though it showed slightly greater dispersion than the linear phase network.

The shunt peaked coupling network has been used in all of the interstage networks of the high-frequency band-pass amplifiers required for the experimental Deltic, and also for both the input and the output terminating networks for the delay-line transducers. Each of the coupling networks was designed to have a half-power bandwidth of 13 Mc/s centered about 33 Mc/s, which resulted in an overall bandwidth through the 7 coupling networks of slightly greater than 8 Mc/s.

The complete wiring diagram for the band-pass amplifier chassis is shown in Fig 10. Because of the low impedance of the transducer output, it was possible to use a high transconductance type 6AH6 tube (V_1) as a first amplifier where the relatively large input capacity made little difference. Type 6AK5 tubes were used for the rest of the amplifier stages. Fixed tuned inductances were used for the plate coils, and the shunt peaking coils were tuned to the resonant frequency by the use of small trimmer condensers. The amplifier was provided with an automatic gain control, the control voltage for which was obtained the self-biased peak detector (V_6) at the output of the band-pass amplifier. The band-pass amplifiers were constructed on a standard three inch by ten and one-half inch aluminum chassis, and interstage copper-foil shielding was used to prevent regenerative feedback, as shown in Fig. 11 Conventional decoupling networks were used in the plate supply lead and in the automatic gain control bus to isolate the separate stages.

It was convenient to incorporate the data insertion gates on this same chassis inasmuch as they could be combined with the output detector stage. The two 6AS6 tubes (V_6, V_7) shown in the schematic were combined to form a four-input gate. The output of the band-pass amplifier is fed to the control

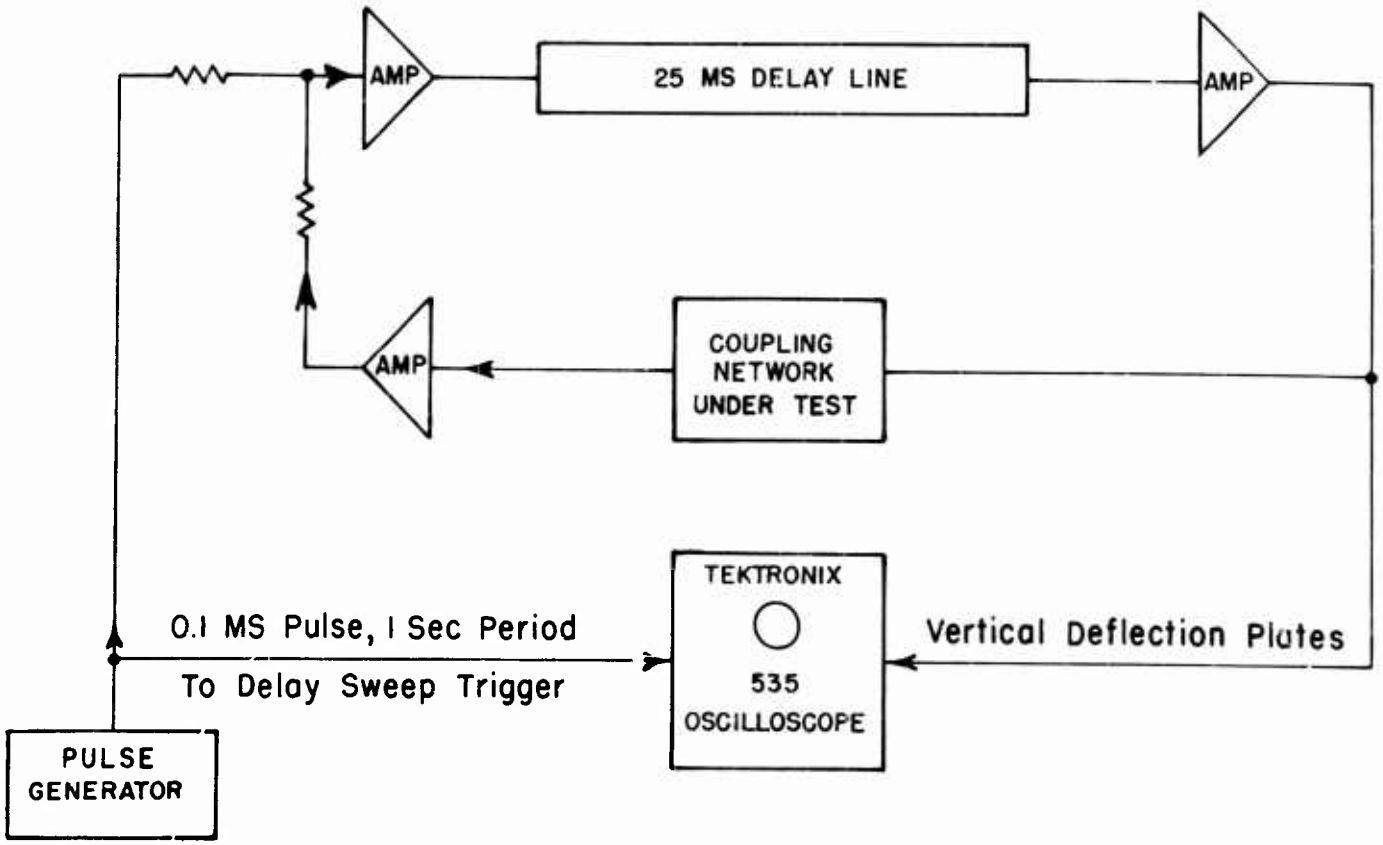


Fig. 8. Block diagram of the interstage network test using the low-frequency delay line model.

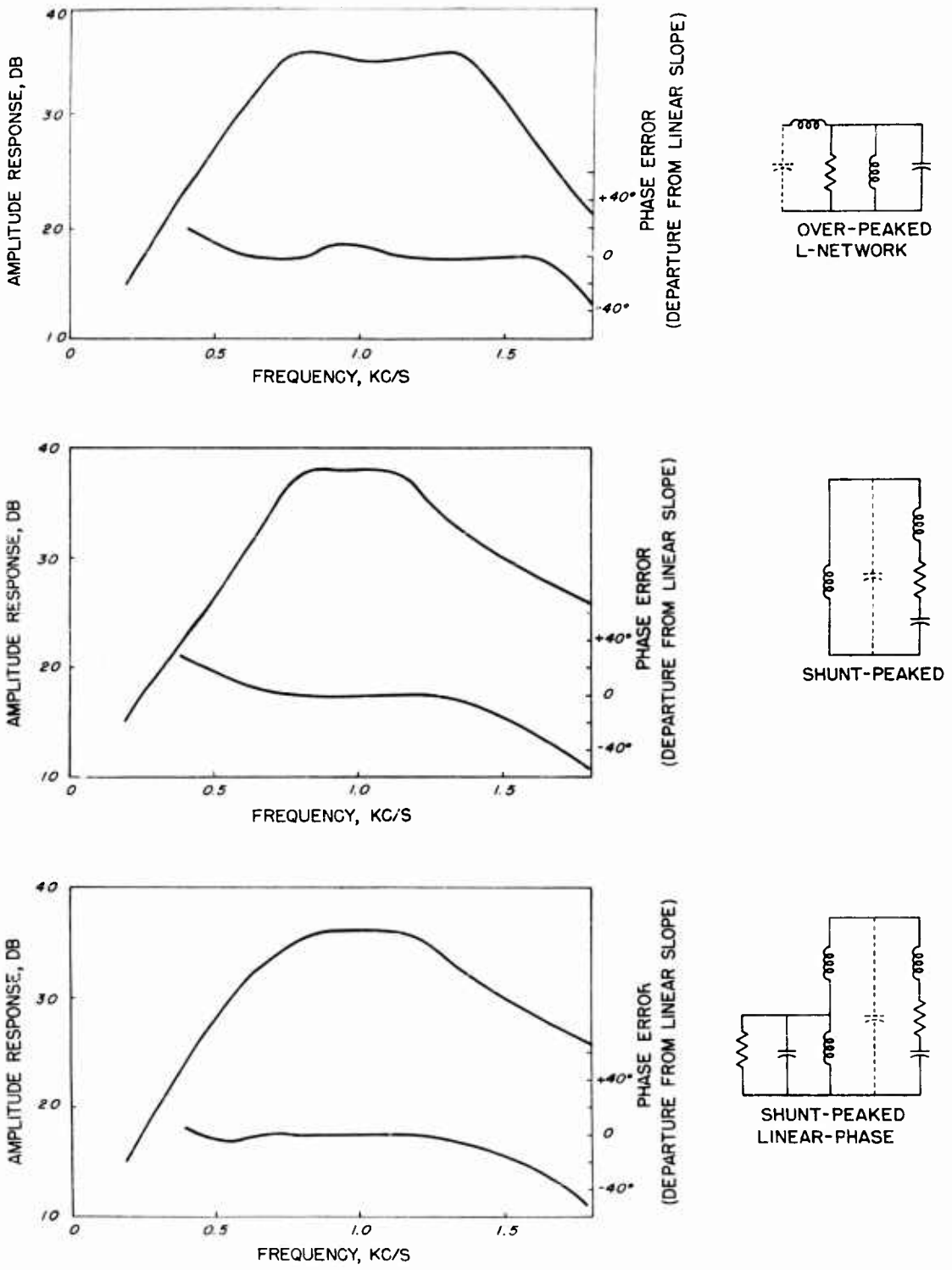


Fig. 9-a. Frequency response and phase linearity of three coupling networks.

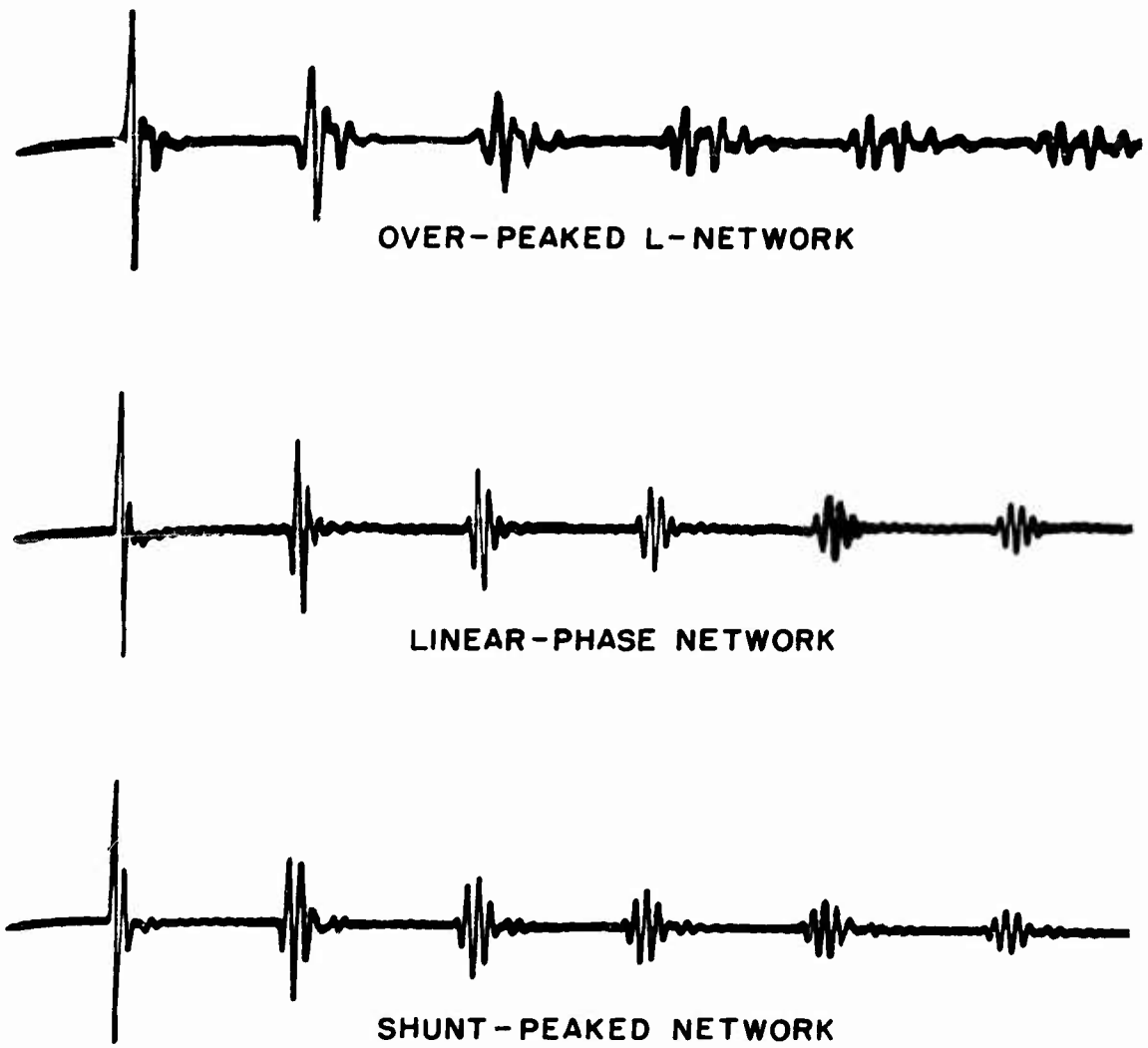


Fig. 9-b. Transient response of the three networks shown in Fig. 9-a.

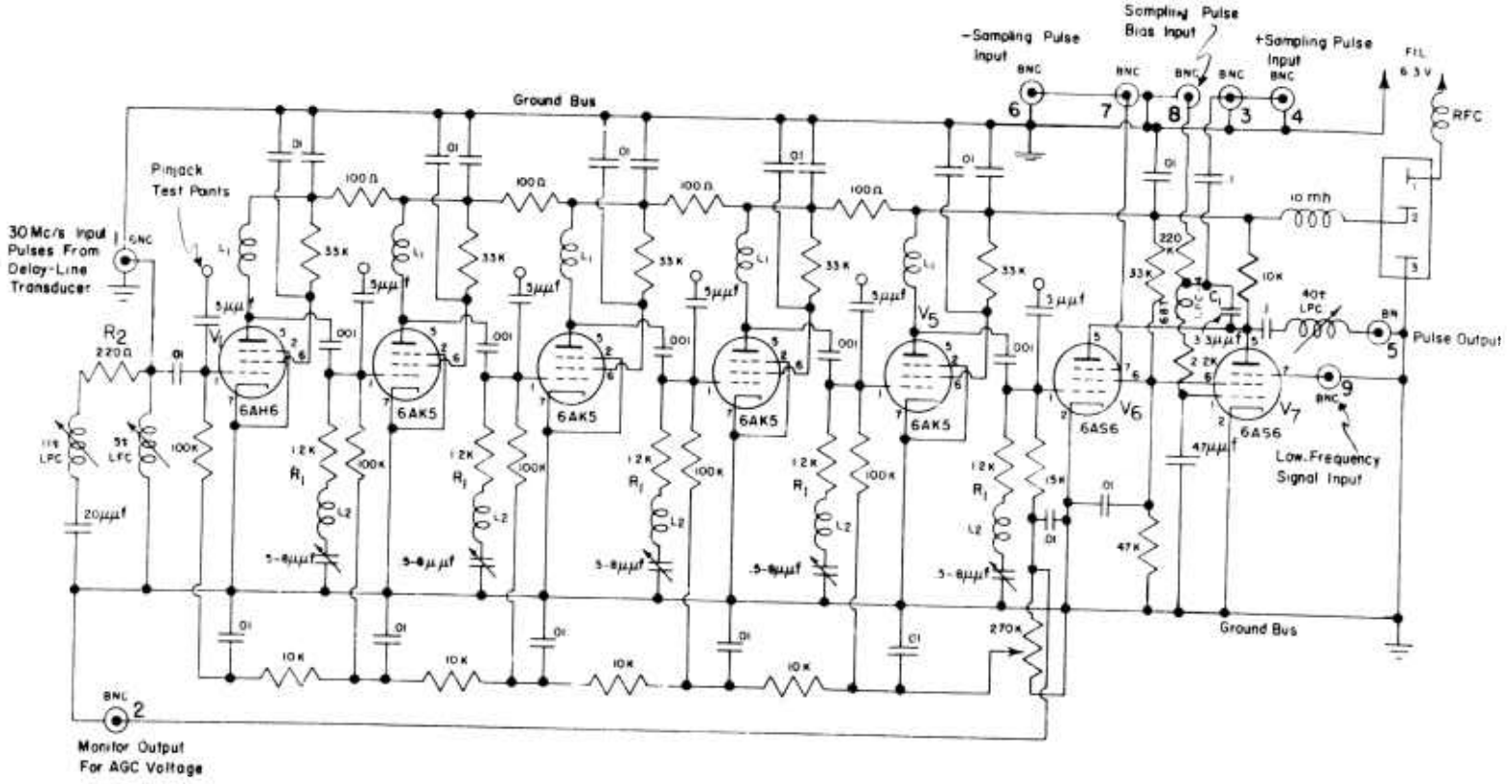


Fig. 10. Wiring diagram of the 30 mc bandpass amplifiers.

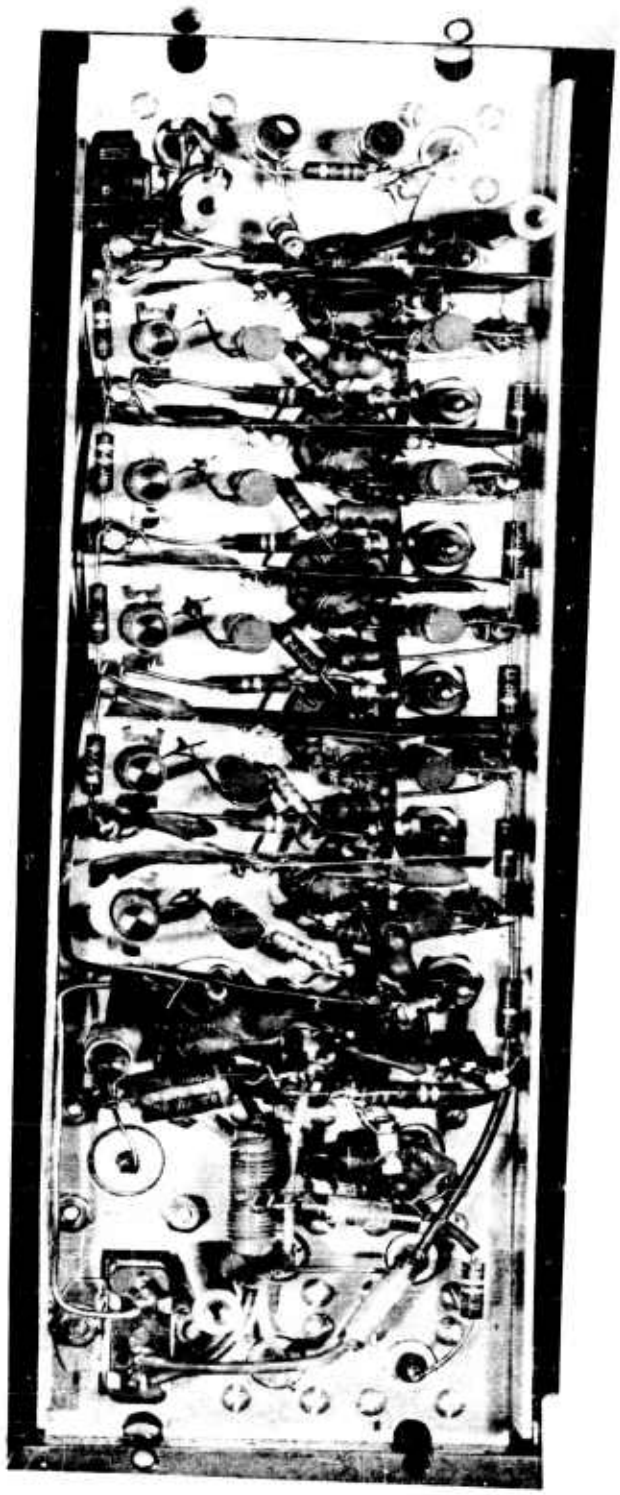


Fig. 11. Bandpass amplifier chassis construction.

grid of one of the 6AS6 (V_6) gating tubes through a grid-leak-condenser bias circuit. The amplitude of the RF pulse input to this grid is sufficient to generate a self-bias of approximately 6 volts which gives a cutoff threshold for the grid signal of approximately 2 volts. A threshold of this magnitude is required to assure cutoff in the absence of an information pulse so that the switching transient of the four-way gate will not interfere with the recirculating pulses which are adjacent to the new data pulse at the time of insertion.

The suppressor grid of this detector-gating tube is used for the erasing gate required in the data insertion process. A negative sampling pulse applied to the suppressor causes complete cutoff of the plate current, regardless of the signal on the control grid. In this way, a pulse is not transmitted through this tube when the sampling pulse is present.

The control grid of the second 6AS6 (V_7) is driven with the positive sampling pulse through an adjustable-bias, capacative-coupling circuit. This adjustable bias permits the amplitude of the current pulse through this second 6AS6 gating tube (V_7) to be matched with that of the current pulse generated by one of the recirculating pulses in the detector gating tube (V_6).

The suppressor grid of this second 6AS6 forms the fourth input to the gate and is fed by the low-frequency incoming signal which is to be sampled. The polarity of this signal determines whether or not the sampling pulse is to be fed into the recirculation loop; thus, it is this tube which carries out the sampling operation on the low-frequency incoming information

The 2,000-ohm delay cable connecting the band-pass amplifier chassis to the recirculation gate chassis forms the load for the plates of the four-way gate. The cable is terminated at the output end only so as to maintain a high impedance plate load for the detector gate circuit, and a peaking coil is inserted between the 6AS6 plates and the delay-cable connector to enhance the rise time of the load combination. The output of the gate is sufficient to generate a 4-volt pulse across the 2,000-ohm cable impedance. A pulse of this amplitude is sufficient to excite the driver tube in the succeeding chassis directly, without further amplification. A small neutralizing capacitor (C_1) is connected between the + sampling pulse input and the detector input to cancel the negative pulse arising from the capacitive coupling between suppressor and plate of the erasing gate (V_6).

D. Reclocking Gate Chassis

The pulse train output of the band-pass amplifier chassis is fed to the reclocking gate chassis through a 2,000-ohm delay cable, the length of which may be adjusted to provide synchronization between the various chassis of the Deltic. This pulse train is amplified in a 6AH6 driver tube to a peak amplitude of 30 volts, and coupled to the suppressor grid of the 6AS6 reclocking gate as shown in the schematic of Fig. 12. Careful attention was paid to the termination of the delay cable at the input of the driver amplifier to minimize the effect of spurious reflections from this length of cable. A terminating network consisting of an empirically modified "T" section of a low-pass filter, having the same characteristic impedance as the delay cable and incorporating the input capacity of the tube as one of its elements was used to neutralize the input capacity of the tube and the shunt capacity of the cable connector and plug over as wide a bandwidth as possible. With this termination, less than 10 per cent reflection was observed at any time.

The reclocking gate driver amplifier (V_1) utilizes a small inductor in series with the plate load to form a shunt-peaked coupling network having moderately fast rise time, and the plate load is tapped to provide an output for the other chassis in the Deltic correlator. The output at this tap is passed through a second amplifier (V_4) whose plate load is the 2,000-ohm cable termination network for the high-impedance interconnecting delay cable used between this chassis and the other chassis to which the signal must be connected.

Since the nature of the information which is to be fed into the pulse train is such that the probability of having less than 30 per cent or more than 70 per cent of the line full of pulses at any one time is very remote, it was possible to use capacitive coupling with a DC restorer diode on the reclocking gate suppressor grid (V_2) to maintain the base line at zero voltage.

The clocking pulse applied to the control grid of the 6AS6 reclocking gate (V_2) generates in the tube a current pulse of very short duration. The suppressor grid exerts sufficient control to deflect the current pulse either to the plate or to the screen grid, thus performing the gating action required. In order to obtain the saturation in the suppressor control characteristic, necessary to stabilize the pulse amplitude, it was found that a reduced screen voltage of approximately 70 volts was required. The effect of reduced screen

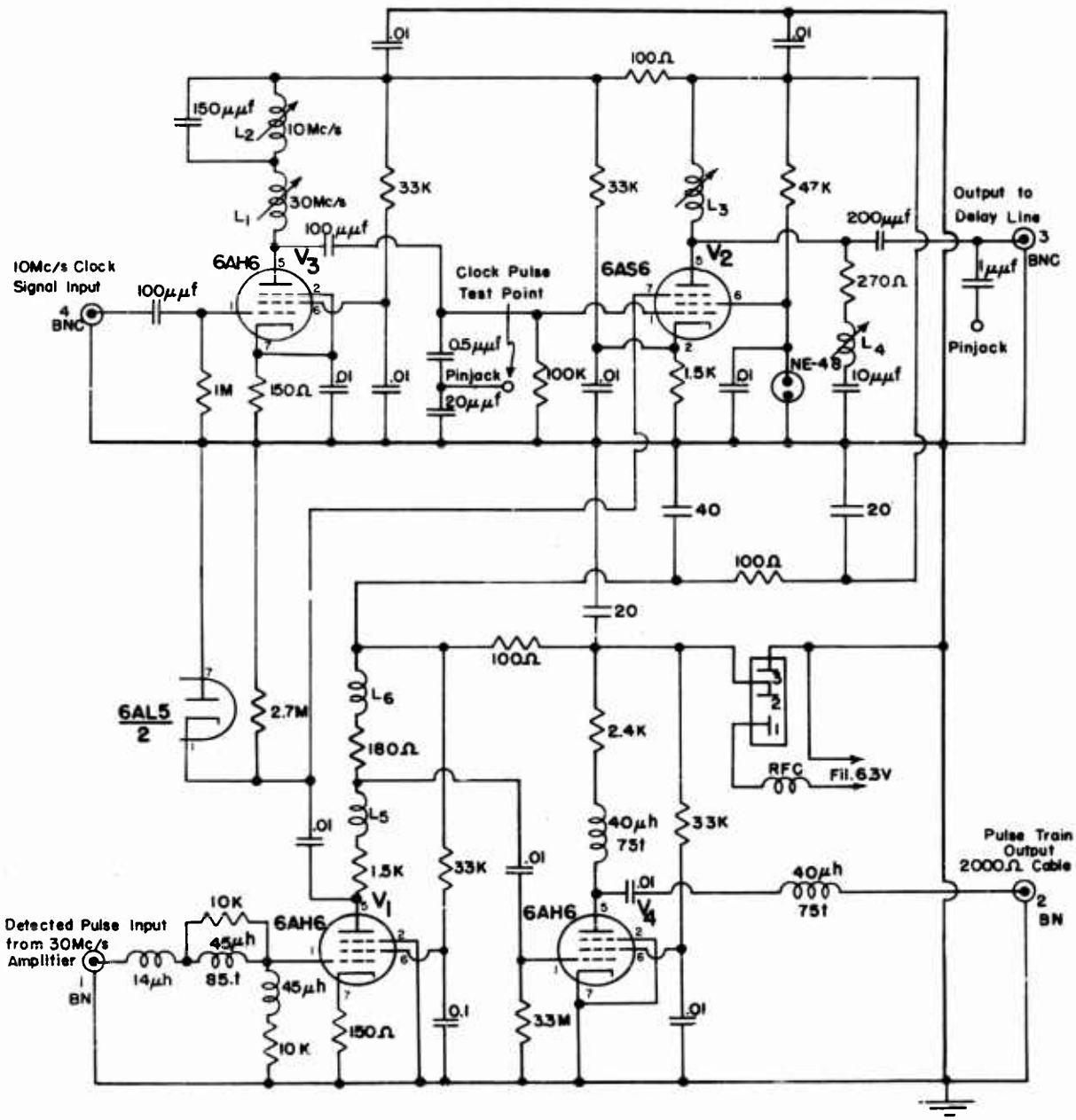


Fig. 12. Wiring diagram of the reclocking gate chassis.

voltage is shown in Fig. 13 where the pulse output on the 6AS6 plate is displayed as a function of the suppressor voltage. It is obvious that the saturation characteristic of the 70-volt screen voltage curve is far superior to that of the 150-volt curve. This flat saturation characteristic compensates for gain changes in the amplifiers and for amplitude variations caused by adjacent pulse interference which arises from the spreading of the pulse in the band-pass amplifier. It also compensates for the amplitude decay of a long pulse train such as occurs when very low frequencies are inserted into the storage loop. Type 991 glow tube regulators were used on the screens to provide the 70 volts of screen voltage at a reasonably low impedance and thus maintain a uniform pulse amplitude independent of short or long term duty cycle.

In checking the saturation characteristics of the 6AS6 tube, considerable variation among tubes supplied by various manufacturers and even before tubes of the same manufacturer was observed. It was accordingly necessary to perform some reasonable selection of the 6AS6 tubes to be used in this recirculating gate. The selection had to be made on the basis of the saturation characteristic rather than on the basis of the transconductance as measured by an ordinary tube checker.

As has been mentioned, the most effective way of providing a well-defined clocking pulse which is short compared to the 0.1 μsec recirculated pulses is to generate this pulse as a current pulse in the reclocking gate tube (V_2) itself, rather than to use an external pulse-generating circuit which, for the rise time involved, would involve the use of extremely low-impedance, high-power circuits. The signal fed into the 6AS6 grid to form the clock current pulse in the tube is obtained from a doubly resonant plate load in the clock pulse amplifiers (V_3). Two resonant tuned circuits were inserted in the plate circuit of a 6AH6 tube to provide the high-impedance circuit necessary for the high-voltage clocking signal. One of these resonant circuits was tuned to 10 Mc/s, and the other was tuned to 30 Mc/s. The impedance ratio of the two tuned circuits was adjusted to give a balance between the first and third harmonics to form a signal of the shape shown in Fig. 16. This clocking signal has a peak-to-peak amplitude of approximately 50 volts, and only the upper three volts are required to drive (V_2) from cutoff to grid conduction,

thereby producing a very narrow current pulse. The first and third harmonics of the 10 Mc/s clock signal are generated in the clock pulse amplifiers (V_3) by over-driving the grid of the tube with a 10-volt, RMS, 10 Mc/s signal applied through a grid leak bias network to the control grid. The construction of the reclocking gate is shown in Fig. 14.

E. Timing Channel

The problem of synchronizing the sampling pulse with the recirculating delay-line memory channel was solved by using a separate timing channel for the generation of this pulse. The timing channel used was identical to the standard recirculation loop as described previously, with the exception of the insertion of a free-running multivibrator (V_5,V_6) between the driver amplifier (V_1) and the reclocking gate (V_2) as shown in the schematic of Fig. 15. This multivibrator, which has a free period slightly longer than the recirculation period of the line, introduces a standard-shape pulse into the recirculation loop which, upon its return, triggers the multivibrator to lock it in to the recirculation period of the line. The on-off periods of the multivibrator are made approximately equal so that the circuit will be insensitive to any spurious pulse arriving within one half of the recirculation period behind the main triggering pulse. In this way, it is impossible to have more than a single pulse recirculating in the line at any one time; and, of course, it is also impossible to have less than one pulse in the line since, in the absence of a pulse, the multivibrator will "free-run" and thus insert a starting pulse in the line.

A shorted section of delay cable is used in the output plate circuit of the multivibrator (V_6) to shape the pulse inserted into the reclocking gate. The 0.1 μsec sampling pulse is obtained from a tap near the end of this delay line stub, and is fed to a phase splitter (V_4) to generate both the positive and the negative sampling pulses required for the new information gate. A 6CL6 is used for this phase splitter because of its high peak cathode current and relatively high transconductance. The phase splitter is biased past cutoff so as to reject the low-level reflections caused by the capacitive impedance mismatch at the tap on this delay line.

The length of the delay-line stub is adjusted to locate the leading edge

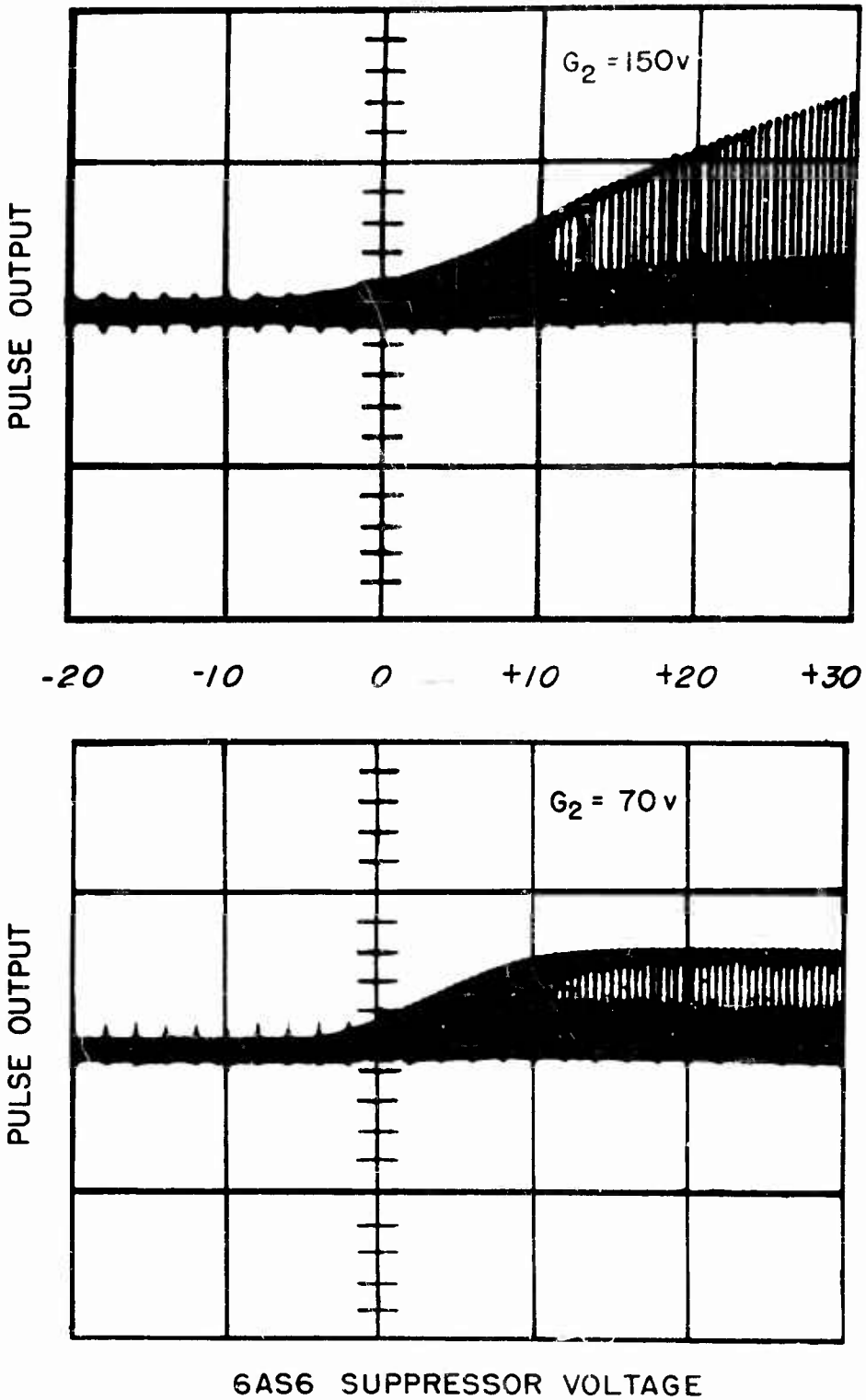


Fig. 13. Gating characteristics of the 6AS6 reclocking gate for two values of screen voltage.

Fig. 14. Reclocking gate chassis construction.

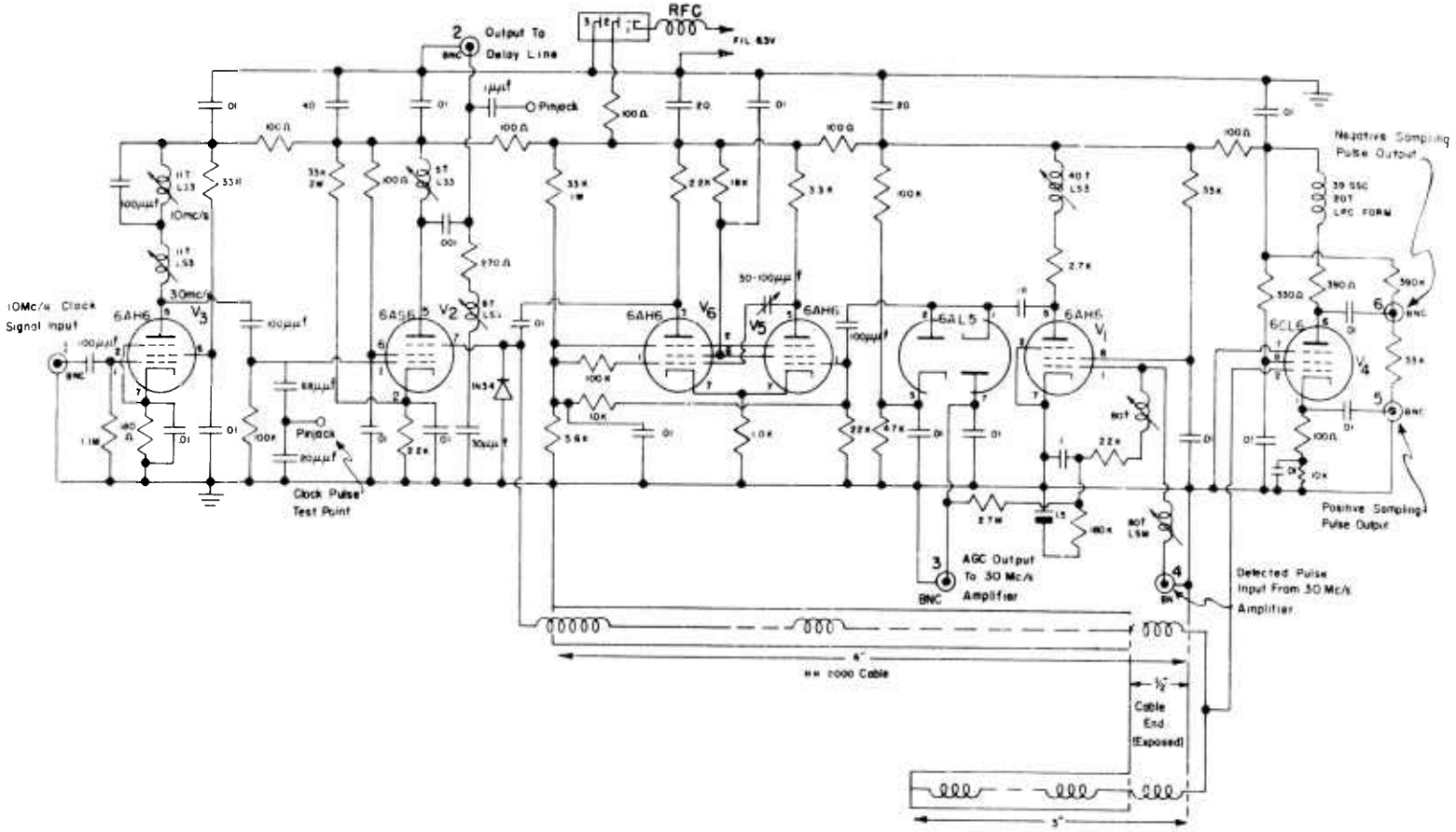


Fig. 15. Wiring diagram of the timing-channel reclocking gate.

of the pulse applied to the reclocking gate midway between two clock pulses. The relative phase of the clock pulses, recirculated pulse, and sampling pulse are shown in the scope traces of Fig. 16.

The construction of the timing channel reclocking chassis is shown in Fig. 17. The delay cable used for pulse-shaping is shown at the left of the chassis, and the trimmer capacitor for controlling the multivibrator period (the only adjustable control on this chassis) is located near the center.

F. Clock Oscillator

The timing channel, described in the previous section, is the primary time standard for the entire Deltic correlator. The clocking signal must be locked in phase to the sampling pulse. In order to accomplish this, an automatic frequency control circuit is incorporated in the clock oscillator chassis, as shown in the schematic of Fig. 18. The AFC signal is derived from a phase detector which compares the phase of the sampling pulse with the phase of one of the clocking pulses. The phase detector consists of a 6AS6 gating tube (V_2) used in a circuit similar to the reclocking gate of a memory channel. The difference lies in the plate circuit, where a resistive load is used instead of the tuned band-pass circuits. The narrow pulse appearing on the plate is converted to a DC control voltage by a peak detector (V_7), and after suitable filtering is applied to the control grid of the reactance tube, which is shunted across the oscillator (V_9) tank circuit. The control characteristic of this circuit is illustrated in Fig. 19. The curve was obtained by breaking the automatic frequency control circuit at the point marked "X," and applying a variable voltage to the reactance tube while observing the AFC bias output delivered by the AFC detector (V_7). As indicated by the curve, the circuit exhibits very sharp control characteristics, and phase errors of less than 1/10th of a pulse period or digit interval may be expected over a wide range of operating conditions.

This reactance tube exhibits a sufficient range of control to vary the frequency over a range which encompasses several different multiplication factors, differing by integers, which will satisfy the phase condition required by the AFC system. These multiplication factors, the N of Chapter II, may take on whatever value is required to satisfy the phase condition without otherwise

affecting the operation of the Deltic or influencing the characteristics of the correlator sweep. It is this flexibility which permits the use of unregulated temperature enclosures for the delay lines of the various memory channels which must be synchronized. The only requirement is that the various lines be maintained at the same temperature with respect to each other, the absolute temperature being unimportant.

If, or when, temperature drift of the delay lines or frequency drift of the oscillator carries the clock oscillator control beyond the limit of its control range, the control may be reset to one of the "allowed" frequencies by a push button switch provided on the control panel (Section L). This switch resets the automatic frequency control voltage to some predetermined reference, whereupon, after release of the push button, the automatic frequency control selects the nearest "allowed" frequency mode and controls at that voltage.

The output of the clock oscillator is coupled to the various chassis through a cathode follower (V_{10}). Incorporated on the clock oscillator chassis is an amplifier (V_5) for the sampling pulse which acts as a pulse-stretcher providing a suitable signal for the frequency divider chassis.

G. Frequency Divider Chassis

The output pulse of the clock oscillator just mentioned is fed to a 32:1 binary scaler, Fig. 20, and then to a 10:1 scaler which uses a glow-transfer type counter tube, Fig. 22. This gives a total frequency division of 320:1 to provide the time base for the correlation sweep.

At the count of 320, it is necessary to obtain from the output of the frequency-divider strip a transfer pulse which has the duration and phase of a single repetition period in the memory channel, 30.7 μsec This is obtained by a series of summing and clipping operations on the outputs of the various stages in the divider. The output of the first stage of the 32:1 divider chassis (V_1) is a square wave having a period of 61.4 μsec, with the beginning and end of the positive swings synchronized with the sampling pulse. The first summing and clipping operation is performed to select one out of 16 of the positive cycles of this square wave. The summation bus is connected by a 2.2-meg resistor to one of the plates of each counter stage as shown in the

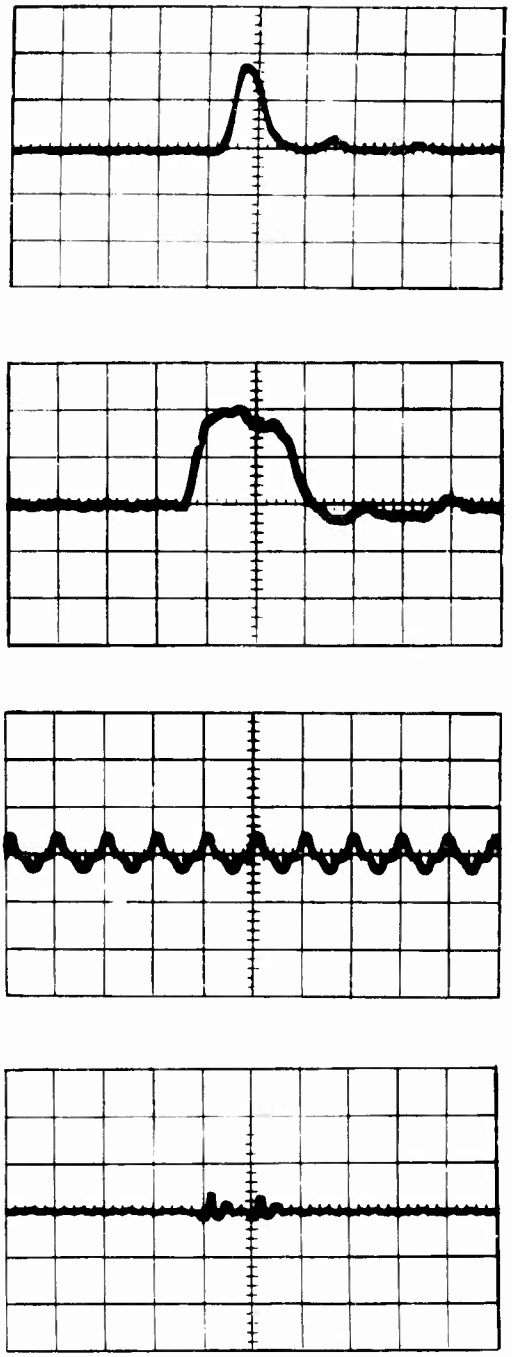


Fig. 16. Wave forms and relative phase of signals appearing in the timing-channel reclocking gate.

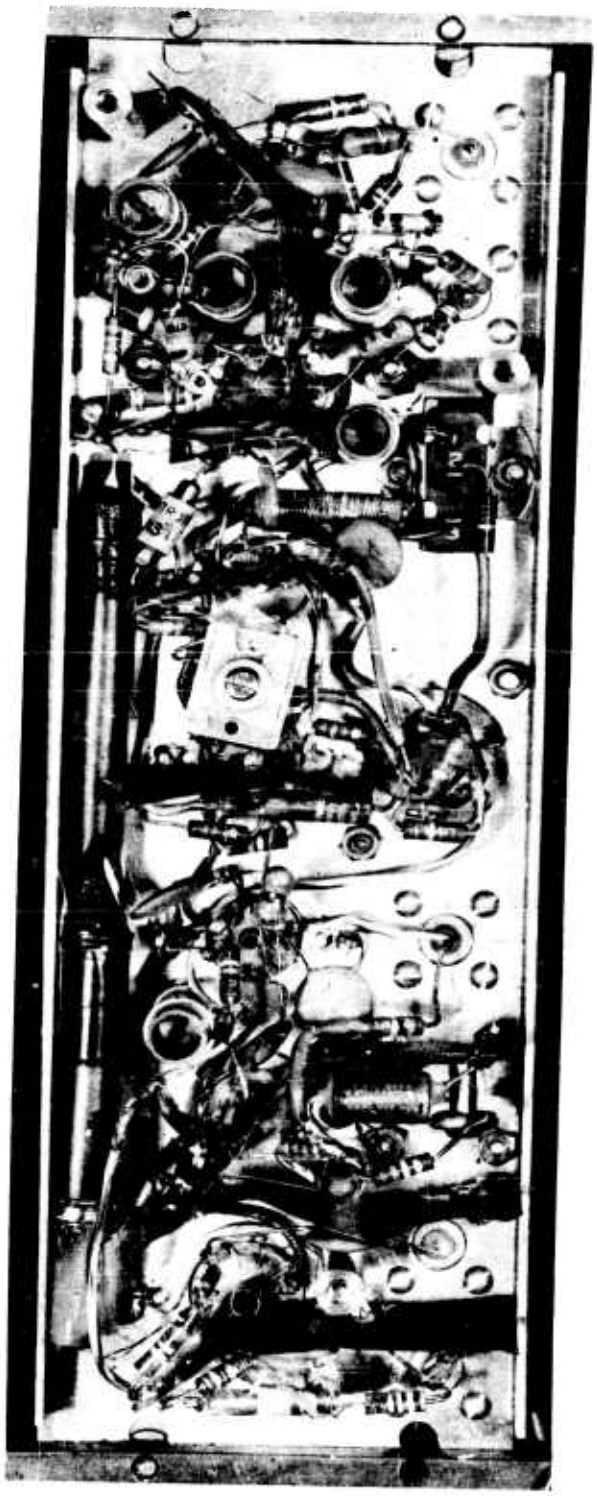


Fig. 17. Timing-channel reclocking gate chassis construction.

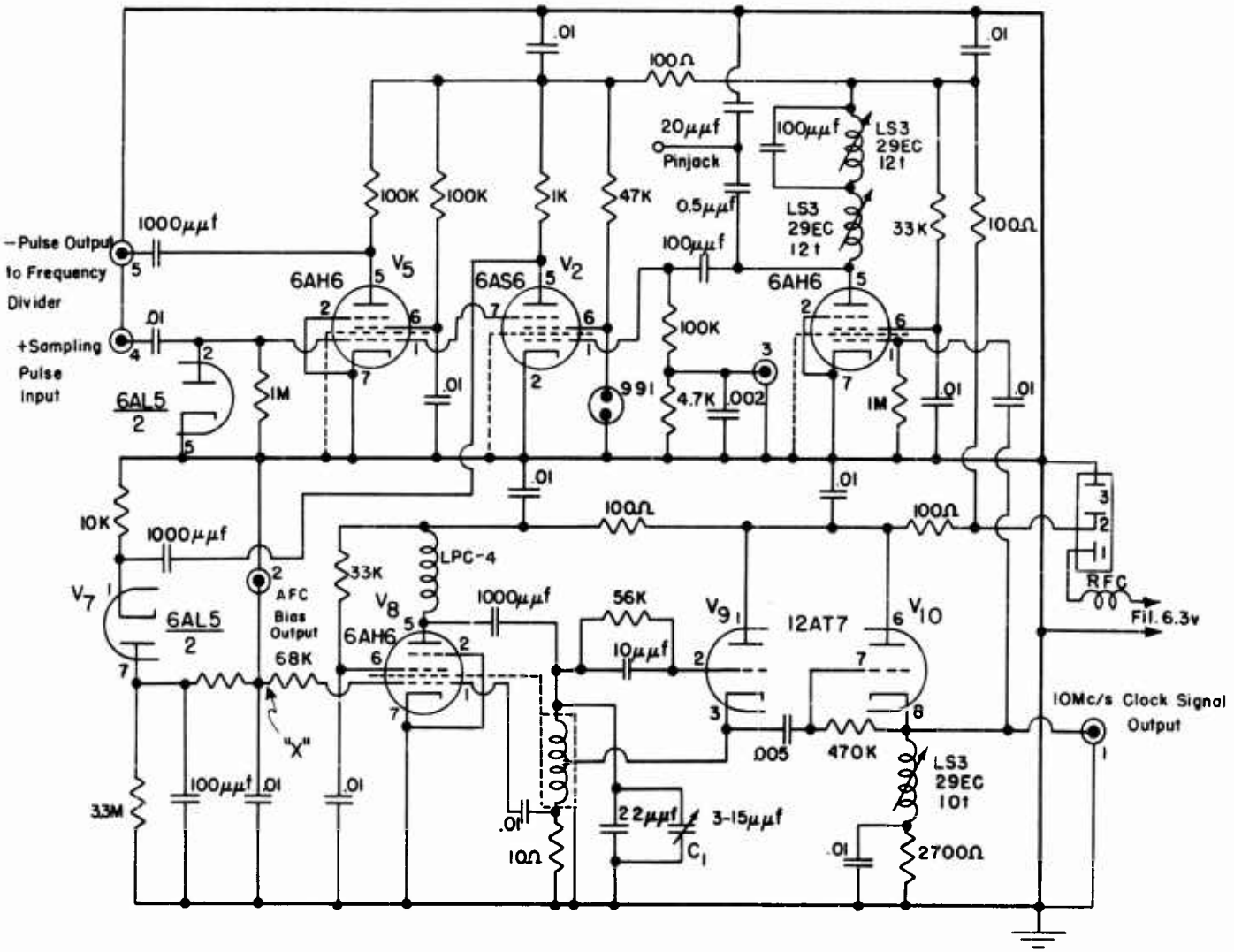


Fig. 18. Wiring diagram of the clock oscillator chassis.

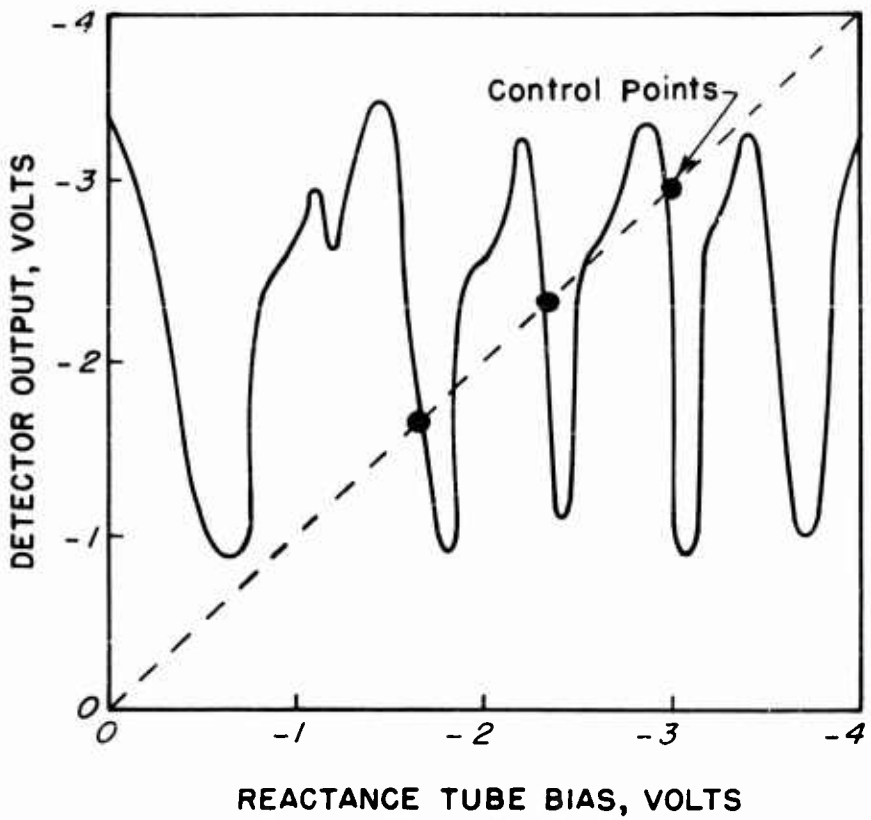


Fig. 19. AFC control characteristics of the clock oscillator.

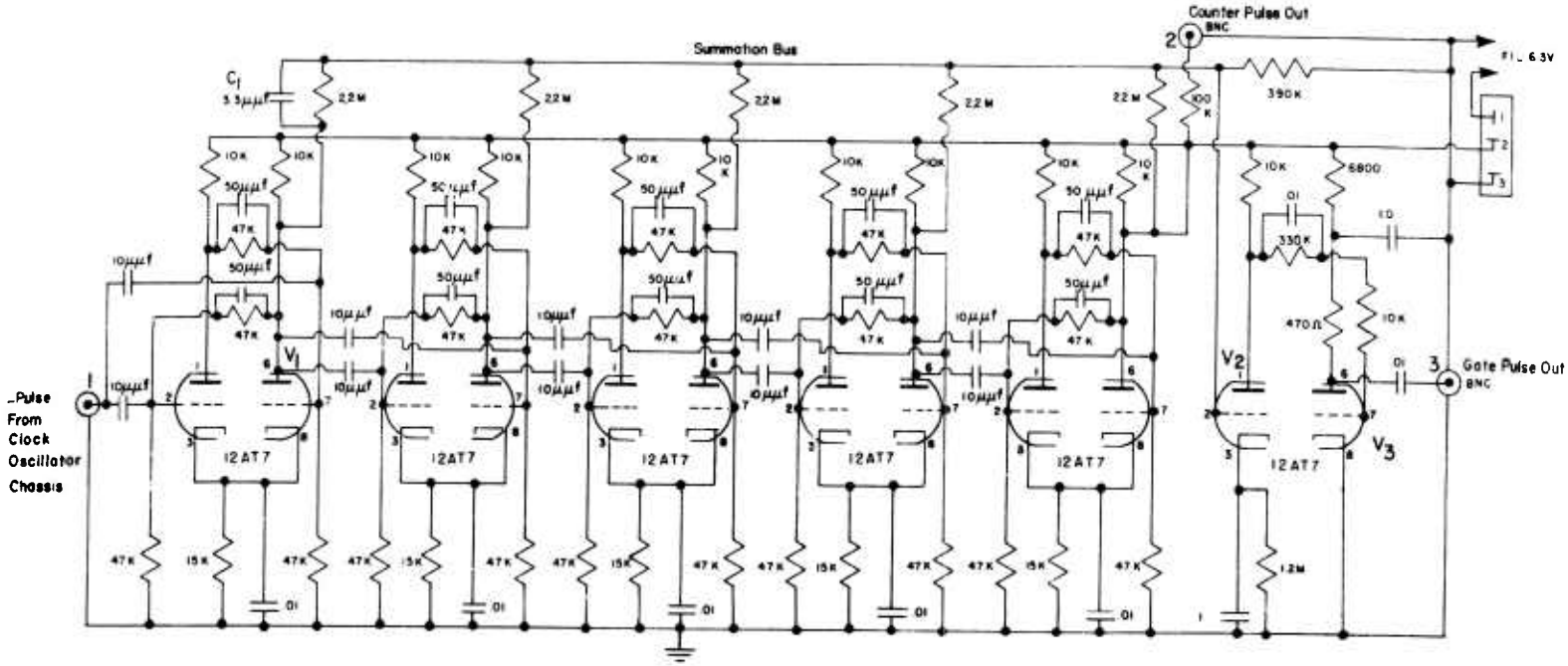


Fig. 20. Wiring diagram of the 32:1 frequency divider chassis.

schematic of Fig. 20. The resulting waveform has five discrete voltage levels as shown in Fig. 21, corresponding to the various possible combinations of the outputs of the five binary stages. This signal is periodic with a period of 32 x 30.7 μsec or 0.98 ms, and it can be seen that during this interval, there is a single pulse which rises above all the rest. The leading and trailing edges of this pulse are sharpened by the addition of a small coupling condenser (C_1) across the coupling resistor between the plate of the first stage and the summation bus. By feeding the summation signal into a self-biasing peak-clipper (V_2), this single pulse may be separated from the composite signal and reshaped by the input and output coupling networks of (V_3) to provide a square gate pulse 30.7 μsec in duration, occurring at a repetition period of 0.98 ms as shown in the lower trace of Fig. 21.

In addition to this gate pulse, the output of the last stage, a square wave of 0.98 ms period, is brought out to a connector to serve as a trigger pulse to the next chassis, the 10:1 divider (Fig. 22).

This trigger signal operates the GS10C glow-transfer counter tube (V_3) driver stage, which consists of a dual triode (V_1,V_2) in a circuit designed to provide a pair of pulses to the transfer electrodes of the counter tube. In the operation of the counter tube, only a single glow discharge may be maintained between the circular center anode and any one of the 30 wire electrodes surrounding it. The 30 electrodes are arranged in 10 sets of 3 each; one of each of the sets is brought out to a pin on the tube base (pins 1 to 10), and is connected to ground either through a resistor, or directly, depending on whether or not an output voltage is desired when the glow is located on this particular cathode. The second electrodes of the sets are tied together and brought out to one pin (12) of the tube to form the first transfer electrode, and the third electrodes of the sets are brought out to another pin (11) to form the second transfer electrode. The anode pin (13) is connected through a limiting resistor to a high-voltage supply to maintain a nearly constant-current glow discharge in the tube. Upon the arrival of a trigger pulse to (V_1), a negative pulse is applied to the first transfer electrode from the plate of (V_1) and the glow discharge transfers from the particular cathode it was on to the first transfer electrode adjacent to it. Shortly before the end of this pulse, a negative pulse appears on the second transfer electrode from the

plate of (V_2) so that the glow is transferred to it at the end of the first pulse. At the end of the second pulse, the glow moves to the nearest cathode (the one belonging to the next set of three electrodes) because it is then more negative than either of the transfer electrodes. This transfer sequence occupies an interval of approximately 200 μsec. During the remainder of the trigger period, approximately 800 μsec, the glow remains on a cathode electrode. Thus, it can be seen that a pulse 0.8 ms long appears across the resistor in series with cathode number 1 every 10 trigger periods or 9.8 ms. This pulse is mixed with the gate pulse having a 0.98 ms period and a 30.7 μsec duration appearing at the output of the 32:1 divider chassis in an RC mixing network and introduced into a self-biased peak-clipping circuit (V_4) to select one out of every 10 pulses, thereby obtaining the transfer pulse. The waveforms of the input and output of this mixer circuit are shown in Fig. 23. It was necessary to use a floating grid in this peak-clipping tube because of the very short duty cycle of the pulse. The use of a floating grid does not cause any difficulty in circuit stability inasmuch as the tube is driven from grid conduction to well beyond cutoff.

The transfer pulse is amplified in (V_5) to form the + transfer gate pulse, and inverted by (V_6) to provide the negative gating pulse, both of which are required for the operation of the storage channel. A positive bias of approximately +10 volts is provided for the negative transfer pulse output. In this way, the suppressor grid of the erasing gate is operated in the saturation region to avoid any amplitude instability which might arise from base-line shifts of the transfer pulse, and also to obtain maximum current out of the detector stage during the storage interval. A cathode follower (V_7) operating from the + transfer pulse provides a synchronization pulse for the oscilloscope display.

The frequency-divider chassis also provides a 100 c/s output for the synchronization of the dielectric recorder drum motor. To obtain this signal, 5 consecutive individual cathodes of the dekatron counter tube are tied together across a single resistor. In this way, a sequence of 5 pulses is obtained when the glow falls on these five cathodes in succession followed by a blank interval of 5 counts while the pulse is on the other cathodes of the counter. This pulse train is passed through an LC filter to provide a reasonably pure 100 c/s sine-wave output, shown at the bottom of Fig. 23, as required by the hysteresis motor for synchronous operation.

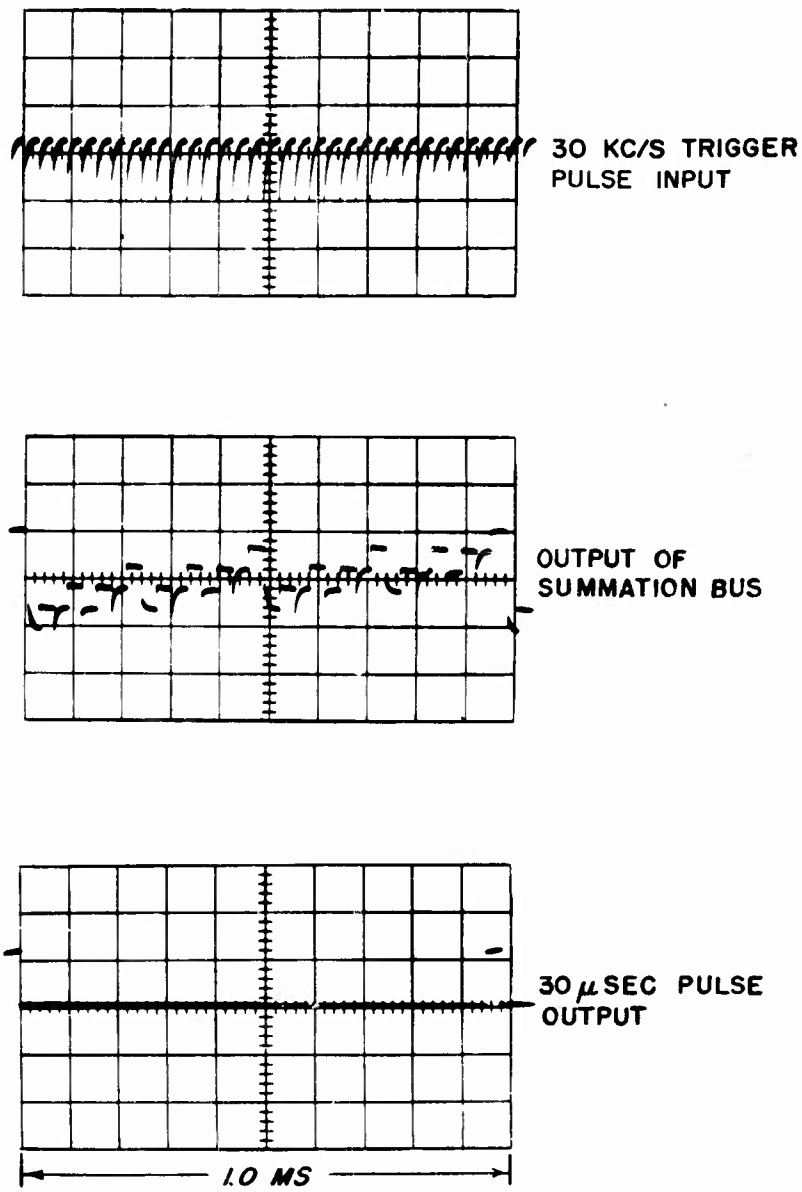


Fig. 21. Wave forms appearing in the 32:1 frequency divider chassis.

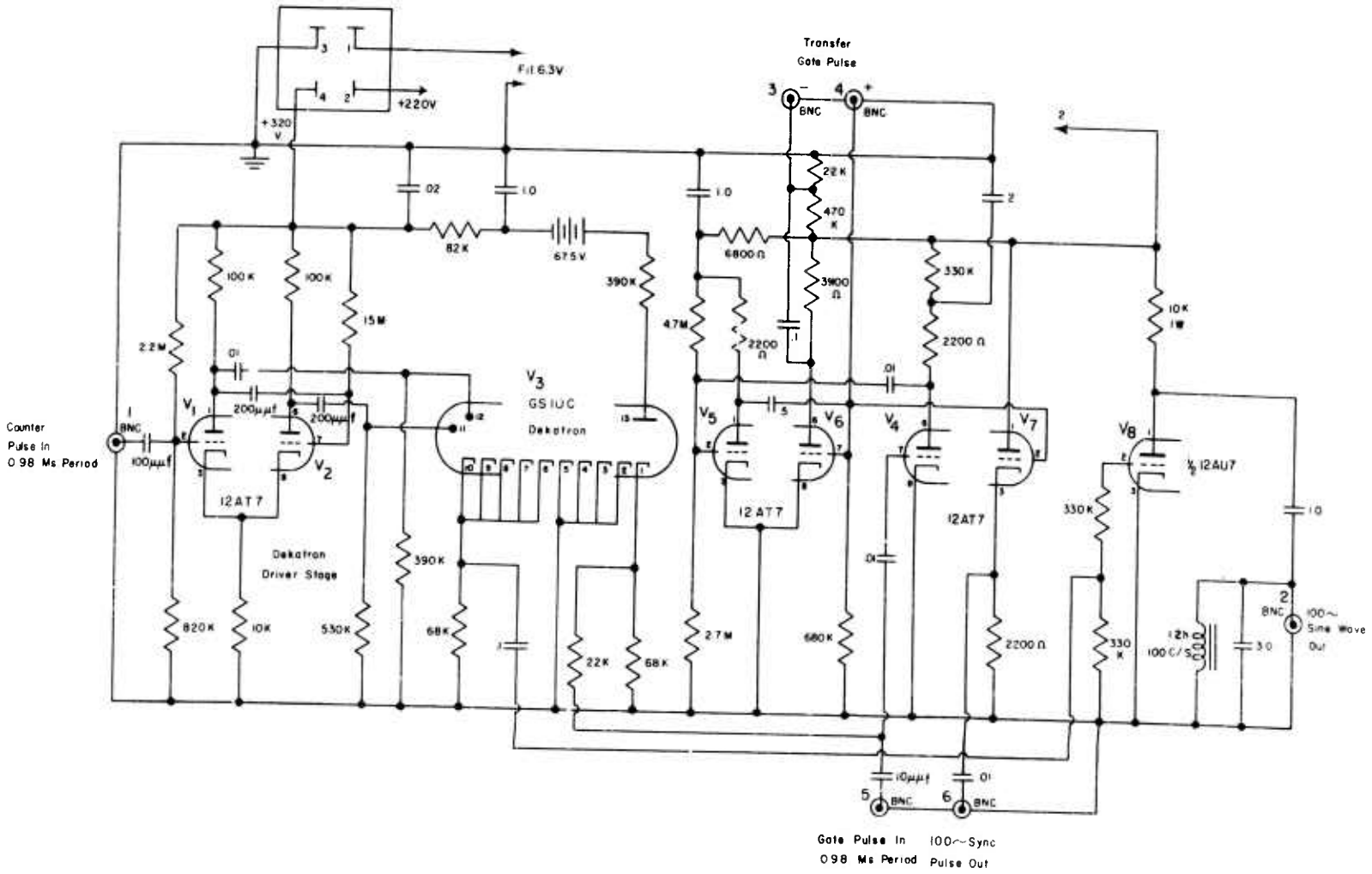
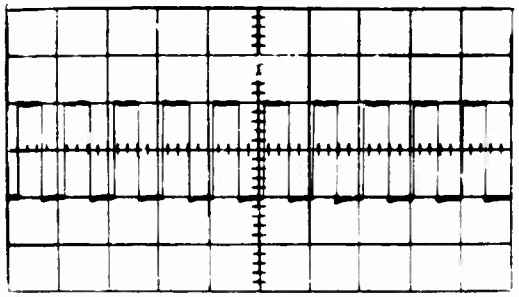
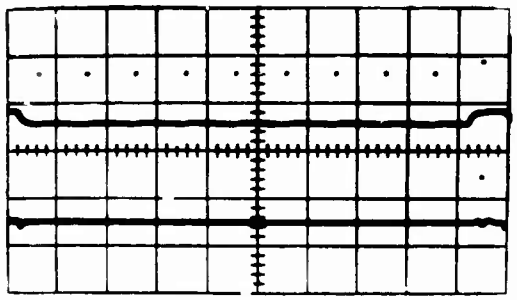


Fig. 22. Wiring diagram of the 10:1 frequency divider chassis.

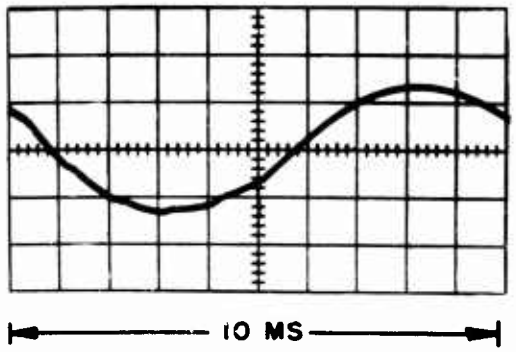


TRIGGER INPUT



MIXER OUTPUT
(30 μS 1 KC/S PULSES +
1 MS 100 C/S PULSE)

30 μS 100 C/S
TRANSFER PULSE OUTPUT



100 C/S SYNCHRONIZING
SIGNAL TO MOTOR AMPLIFIER

Fig. 23. Wave forms appearing in the 10:1 frequency divider chassis.

H. Storage Channel

The storage channel used in the Deltic is quite similar to the sampling channel. One difference, however, is the addition of an extra 0.1 μsec of delay in the interconnecting cable, thus providing an additional digit of delay in this channel, the need for which was noted in the discussion of Chapter II. Another difference is the manner in which information is introduced at the new information gate (V_7) of Fig. 10.

The latter change is dictated by consideration of the frequency components of the various inputs to the gates. In the sampling channel, previously discussed, the short 0.1 μsec sampling pulse is fed into the control grid of the new information gate (V_7) and is effectively isolated from the plate of the same tube by the shielding effect of the screen and suppressor. The low-frequency information which is to be gated into the circuit may be fed into the suppressor grid without causing any difficulty due to capacitive pickup in the plate circuit of the tube, even though the suppressor-to-plate capacity is relatively high. This is the result of the slow rise time associated with the low-frequency information.

In the storage channel, however, the information to be gated into the line consists of the high-speed pulse train, which has a spectrum identical to that of the recirculating pulses appearing on the plate. For this reason, it is necessary to isolate this train of 0.1 μsec pulses from the plate circuit by introducing it at the control grid of (V_7) and applying the 30 μsec transfer pulse to the suppressor grid. In this way, the relatively long-term transfer pulse will introduce transients only at the start and stop of the pulse and will not affect the main body of the pulse train as it is introduced into the recirculating loop.

Reasonable precautions must be taken in the insertion of the pulse train at the control grid to assure that there will be no long period droop due to the coupling network, which behavior would cause a distortion of the pulse train and an accompanying loss of information.

I. Coincidence Chassis

The final operation required to obtain correlation functions is the

measurement of coincidences between the pulse train of one of the sampling channels and the pulse train in the storage channel; i.e., to carry out the process illustrated in Fig. 5 of Chapter II. Because of the difficulty of interference between adjacent pulses in either pulse train due to the finite bandwidth of the amplifier and gating circuits, the coincidences of the two pulse trains must be measured during the short clock pulse interval, and the coincidence pulse generated must be independent of amplitude variations in either of the two pulse trains. In other words, it is necessary to requantize the output of the coincidence circuit in much the same way that the pulses were regenerated in the reclocking gates.

An important characteristic of this coincidence circuit which is helpful in design considerations is that once the requantization and coincidence measurement take place, there is no longer any need to retain the high-frequency response in the circuitry. Therefore, high-impedance, low-frequency amplifiers may be used to process the correlation output further. By making use of this property, it is possible to combine the reclocking gates with the required threshold detectors in a circuit composed of two 6AS6 gating tubes.

The two inputs to the coincidence chassis from the sampling channel and the storage channel are tied together at the grids of the two gating tubes used in the coincidence circuit shown in Fig. 24. This forms a summation network in which the amplitude is dependent upon the arithmetic sum of the amplitudes of the two individual inputs. The characteristic impedance of each of the 2,000 ohm delay cables serves as a termination for the other, reflections being eliminated by a suitable termination network in both the sampling channel and the storage channel.

The output of the above summation circuit is illustrated in Fig. 25 where the two separate inputs are shown along with the output of the summation network. An extreme negative swing of this combined pulse train occurs whenever there are pulses simultaneously present in both of the individual pulse trains; (note: because of the inversion of the output amplifier the pulses at this point are negative). An extreme positive swing occurs whenever no pulse is present in either pulse train. Thus, either a positive or a negative swing represents a coincidence. The central region of the combined signal represents an anti-coincidence, i.e., the simultaneous occurrence of a

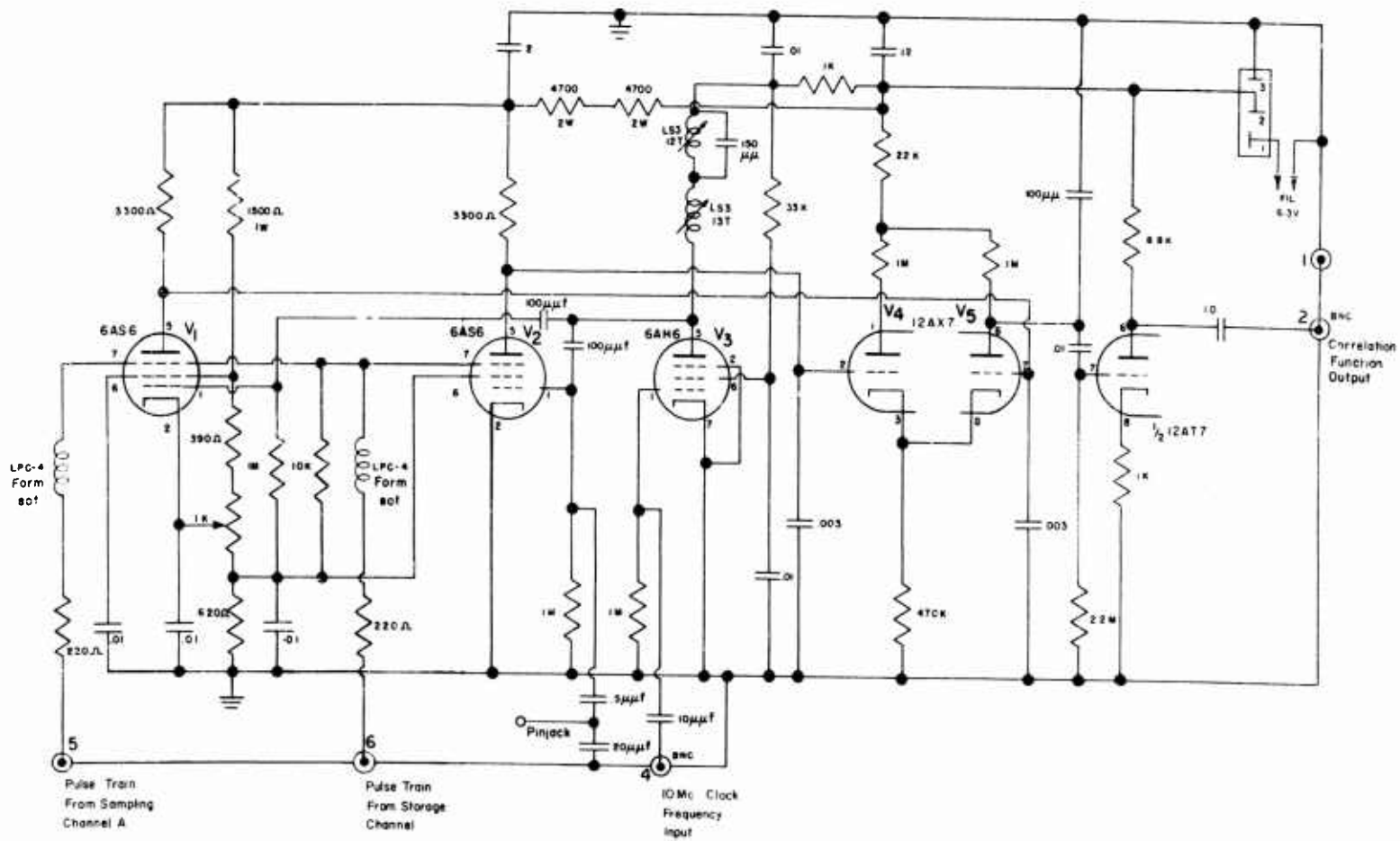


Fig. 24. Wiring diagram of the coincidence chassis.

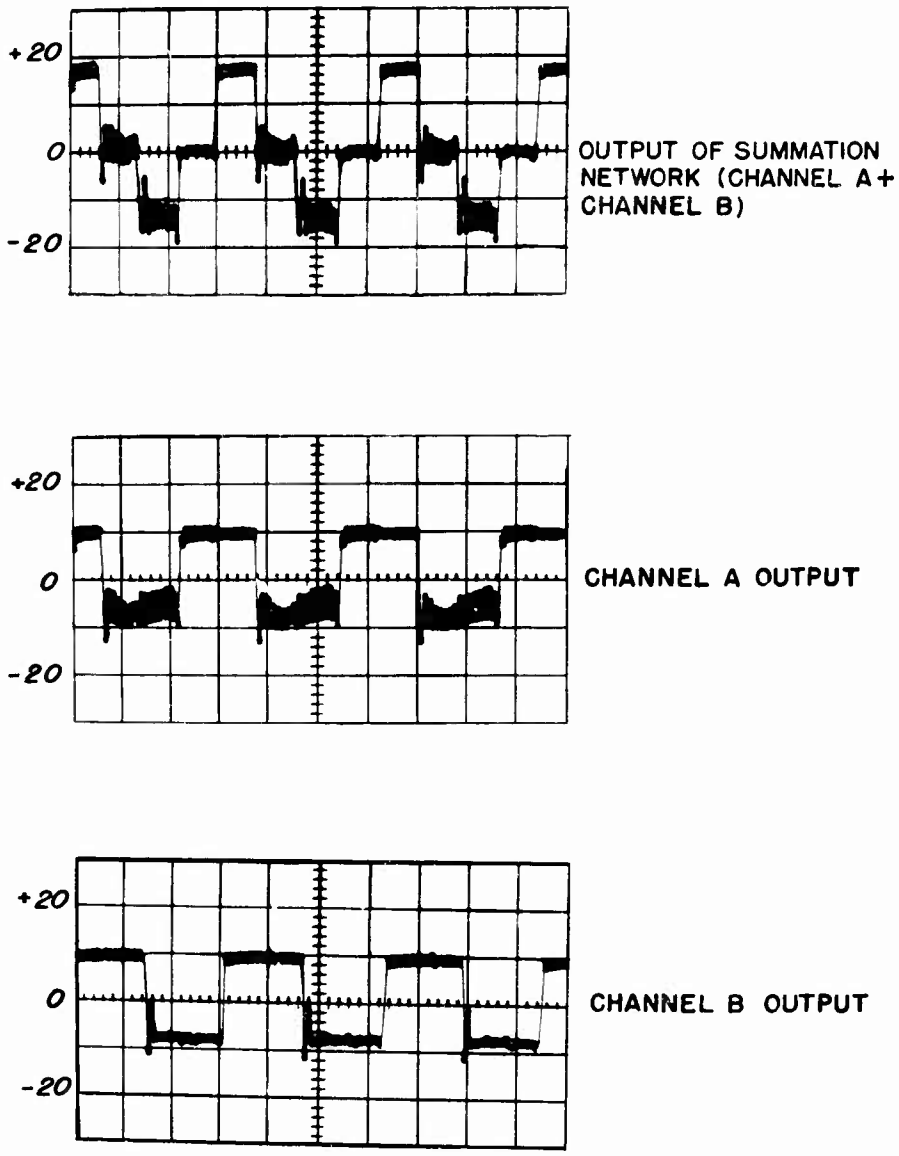


Fig. 25. Inputs and output of summation network.

pulse in either one of the pulse trains, and no pulse in the other. In order to obtain a voltage output representing a coincidence, it is necessary to introduce this combined signal into a circuit having the idealized characteristics shown in Fig. 26a. The usual way of obtaining a characteristic similar to that of Fig. 26a is to use a full-wave clipping rectifier circuit which involves the inversion of the input signal and a clipper on the output. In order to avoid the need of a wide-band inverter stage capable of handling the voltage swings required, it was decided to perform the clipping operation first and then invert at the low-frequency output of the clipper. This is accomplished by operating two 6AS6 tubes (V_1,V_2) (Fig. 24) at a screen voltage of 10 volts and a plate voltage of 50 volts to obtain extremely sharp suppressor-grid control characteristics. The threshold voltages of the two tubes are offset 20 volts by operating the two tubes from a divider network as shown in the schematic. A reclocking signal is fed into the control grid of each of these two 6AS6's from the clock pulse amplifier (V_3), thereby limiting the tube conduction to the duration of the clock pulse and thus performing the reclocking operation required.

When the voltage on the gating grids of (V_1) and (V_2) is above the threshold of (V_1) and below the threshold of (V_2), the current pulse in (V_1) is gated to the plate, but the current pulse in (V_2) is diverted to the screen. When the voltage is above the threshold of (V_2) (20 volts higher), it is also above the threshold of (V_1), and a current pulse appears in both plates. Thus the average plate current in (V_1) is proportional to the number of "no-pulse" coincidences plus the number of anticoincidences, while the plate current in (V_2) is proportional to only the number of "no-pulse" coincidences. A voltage representing the number of anticoincidences is obtained by subtracting the average output of (V_2) from the average output of (V_1) in a differential amplifier stage (V_4, V_5). This "anticoincidence" voltage appears on one plate of the differential amplifier. The complement of the "anticoincidence" voltage, which occurs on the opposite plate, is the "coincidence voltage," since there is a fixed number of pulses in the pulse train. The output of the "coincidence" plate of the differential amplifier has the control characteristic shown in the oscillographic record of Fig. 26b, where the output voltage versus a sinusoidal input signal is shown and, as can be seen, approximates the ideal characteristic of Fig. 26a. The time constant in

the plate circuits of (V_1),(V_2), and the differential amplifier, are adjusted to an approximate cutoff of 15 kc/s, corresponding to the maximum frequency expected in the output of the correlator. This gives rise to an integration time constant of approximately 10 μsec which is comparable to the length of one pulse train. The signal appearing at the output terminal of the coincidence chassis is the correlation function displayed for a total time delay sweep of 9.8 ms, with an effective integration time of 9.42 ms. This relatively short integration time gives rise to large fluctuations in the output when the inputs are random noise signals, but is quite adequate when the inputs are periodic.

J. Dielectric Integrating Drum

The extension of the effective integration time of the correlator by the superposition of several of the successive correlation sweeps has been accomplished by using the averaging properties of a dielectric drum recorder. The dielectric recording process used is described in a Marine Physical Laboratory report.* The storage medium used in this recording process consists of a layer of dielectric material mounted on the periphery of a conducting drum. The signal is stored as a varying electrostatic charge on the outer surface of the rotating drum. The properties of the dielectric material used are such that the bound surface charge decay time constant as determined by surface and volume leakage is long enough compared to the required storage time to be considered negligible.

In order to establish the desired charge on the dielectric surface, the conductivity of an ionized gas is used; the gas in this case is air at atmospheric pressure. The ionization is generated by an enclosed RF corona discharge located near the point on the drum to which the charge is to be applied. This ionization forms a conducting path between a recording electrode and the surface of the drum. By use of a suitable geometry in the enclosed surrounding the ionized region, a desirable balance between the concentration of positive ions and the concentration of negative ions may be established so that the net positive or negative charge deposited on the surface is nearly proportional to

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*A Recording-Reproducing System Using a Dielectric Storage Medium, SIO Reference 55-6, University of California Marine Physical Laboratory of the Scripps Institution of Oceanography, 4 January 1955, V. C. Anderson.

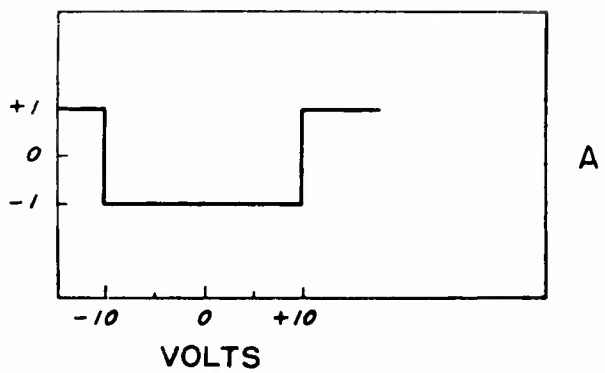


Fig. 26-a. Idealized coincidence circuits.

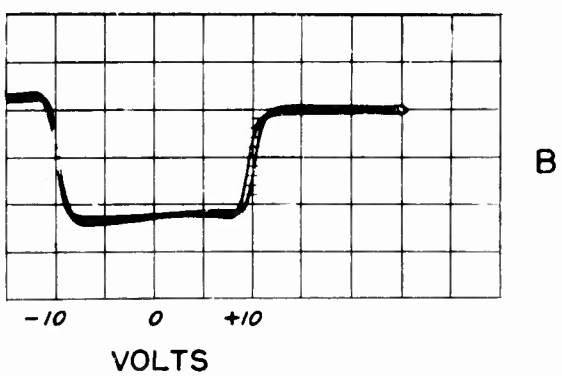


Fig. 26-b. Experimental coincidence circuit characteristics.

the potential difference between the surface of the drum and the recording electrode. Not only the linearity of the conduction characteristics, but also, to an even greater extent, the magnitude of the conductivity may be controlled by varying the geometry of the recording head.

In using the dielectric recorder as an integrating drum, the conductivity of the head is reduced to such an extent that only a small fraction of the charge required to make the surface potential of the drum equal to the applied recording potential is transferred to the drum during the interval in which the surface is exposed to the ionized region in a single drum rotation period. In this way, several passes under the recording head (as many as 10^4) are required to build up the surface potential of the drum to the applied recording potential. Each time an element of the drum passes under the ionized region, an increment of charge proportional to the instantaneous potential difference between the recording electrode and the surface will be transferred. This process is similar to that of charging a capacitor through a resistor, and the build-up of the charge on the drum exhibits an exponential characteristic as does the voltage across the capacitor. Thus, the potential of an element of surface on the drum will be a running time average (a summation with an exponential weighting factor) of the charge increments applied during the prior drum rotations. It may be readily seen that, for a signal which is periodic with the drum rotation period, the charge increments will add up to a large value, while for recording signals which are aperiodic, the charge increments will have random polarities and amplitudes, and the resultant surface charge will tend toward an average of zero. In this way the short-term correlation noise at the output of the correlator which is aperiodic with respect to the correlation sweep period will be greatly reduced, while the small correlation signals which are periodic will build up on the drum to their full value.

The charge pattern which is built up on the drum in this manner is easily reproduced as an electrical signal by observing the induced voltage on a capacitive pickup probe mounted near, but not touching, the surface of the drum.

The construction of the integrating drum is shown in Fig. 27. A 6-inch diameter aluminum alloy recording drum is mounted on the shaft of an Eastern Air Devices synchronous hysteresis motor, and covered with a 0.010"

thick layer of Lucite which serves as the storage medium. The recording and playback heads are fastened to the motor base plate and mounted on opposite sides of the drum. The motor base plate is shock-mounted to prevent motor vibration from reaching the electronic circuits in the Deltic. The Lucite was mounted on the drum by heating a rough-machined Lucite ring (1/16" smaller I.D. than the drum diameter) to the softening point (240°F.) and placing it while soft, over the recording drum. After it had cooled, the outer surface was machined down to obtain the desired 0.010" covering of Lucite.

The hysteresis motor is driven at a speed of 6,000 rpm by a 70-watt driver amplifier whose input is the 100 c/s signal from the 10:1 divider chassis. Operating at this speed, a reasonably true sine-wave output on the amplifier was required to assure true synchronous operation of the motor with no residual slip. Some difficulty was encountered with the operation of the drum because of a small-amplitude hunt which occurs in the synchronous motor. The hunting has a frequency of approximately 1 c/s, and a very low rate of damping. An electro-mechanical damping system would probably be helpful in reducing the amplitude of this oscillation, thereby reducing the possibility of losing high-frequency information when very long time constants are used.

The conductivity of the recording head is controlled by adjusting the mica window slit width with a cam arrangement as shown in the sketch of Fig. 28, so that the integration time constant may be readily adjusted for the particular type of signal being analyzed. The corona discharge which supplies the ionization necessary for the operation of the head occurs at the end of a 0.002" diameter platinum wire which is energized by a high RF voltage (2,000 to 2,500 V rms). The RF coupling to the platinum wire is achieved by making use of the shell-to-core capacitance of the metal-to-glass hermetic seal which serves as a mechanical support for the electrode. The AF potential to be recorded is applied to a ring electrode mounted between the corona discharge and the mica window; ion conduction to this electrode maintains the average potential of the discharge region at the applied recording potential.

The recording head assembly is mounted so that a 0.005" separation between the mica window and the surface of the drum is maintained. This separation is close enough to reduce the diffusion of the ions as they leave the slit and progress toward the drum surface, and at the same time assures

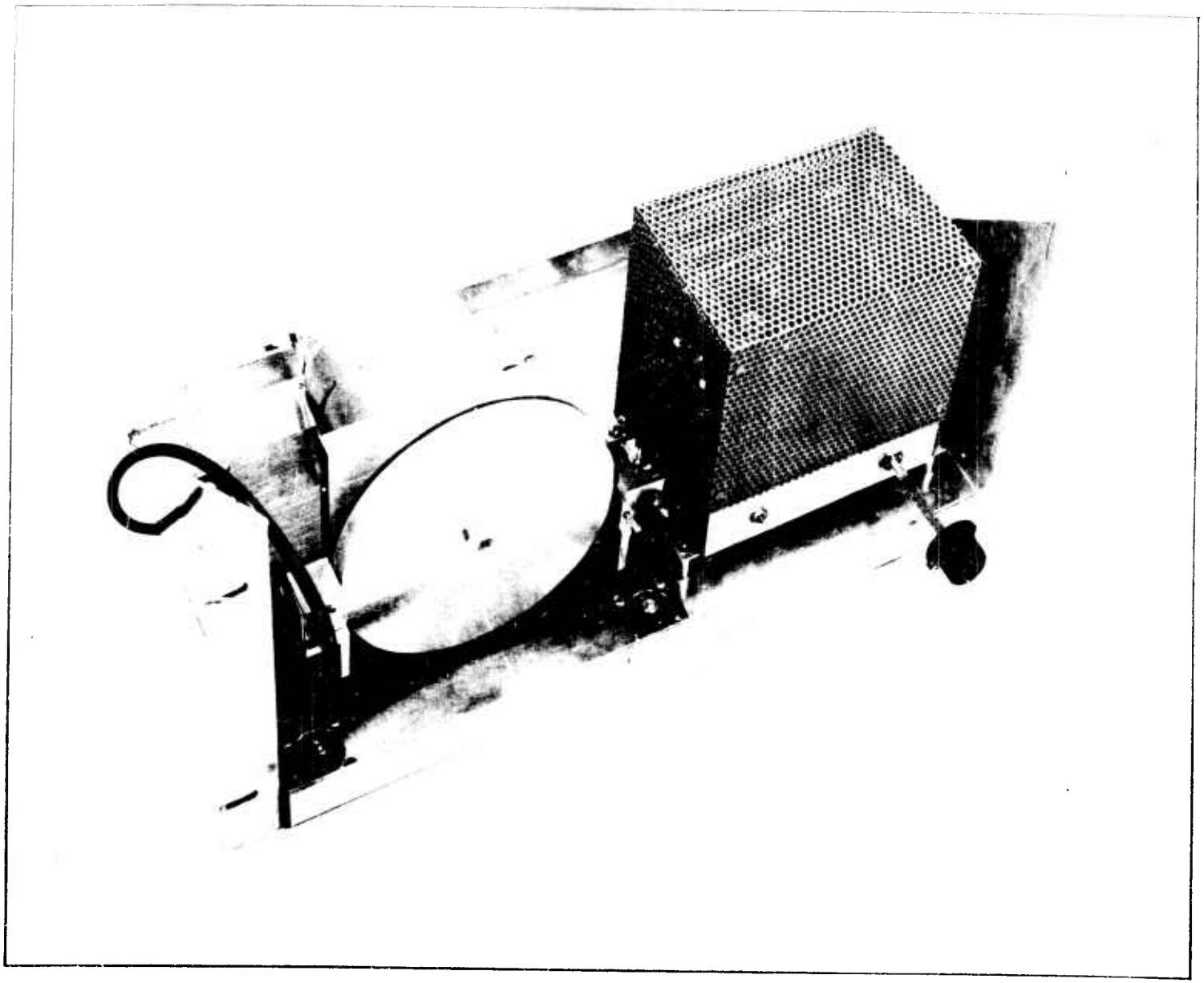


Fig. 27. Construction of the dielectric recorder integrating drum.

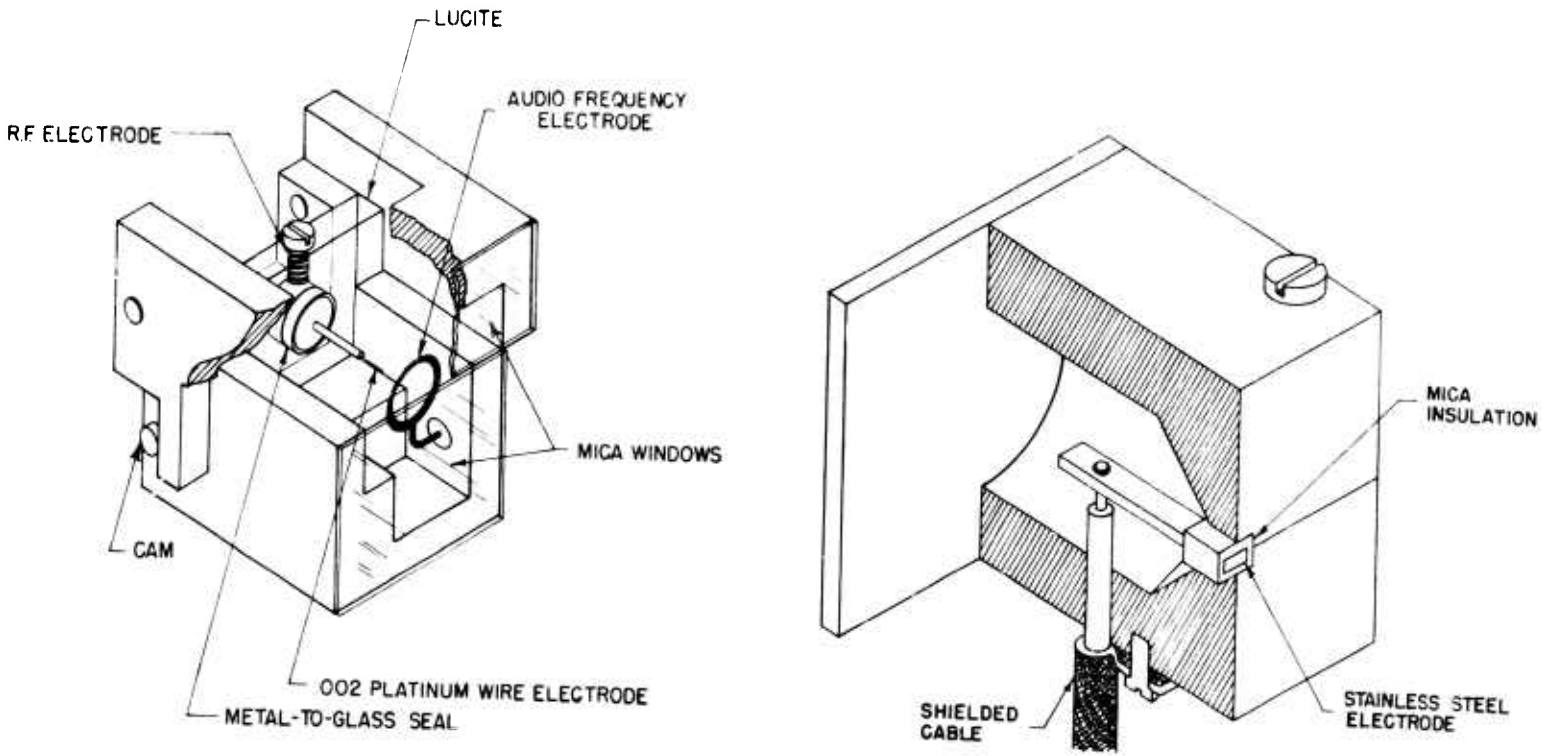


Fig. 28. Construction of the recording head and playback head.

sufficient clearance so that no portion of the window physically contacts the drum at any time.

The playback head consists of a capacitive pickup probe as shown in the sketch of Fig. 28. This probe is shielded on either side by a grounded conductor so as to define the region of capacitive pickup and enhance the short wavelength response of the recording system. The pickup lead is fed to the grid of a pentode amplifier which acts as a voltage amplifier and builds the output up to a useable level.

A schematic of the recording amplifier and the playback amplifier is shown in Fig. 29. The recording amplifier is built on a small sub-chassis mounted on the main support chassis for the dielectric recorder to reduce the possibility of RF pickup in the other circuits in the Deltic correlator. The recording amplifier is composed of two parts: the RF supply which provides excitation power for the corona ionization source is constructed around a Miller Type 4524 RF transformer, a commercially available coil used in high-voltage cathode-ray tube power supplies. The driver amplifier, supplying the potential to be recorded, uses a high-impedance, crystal-cutter transformer to generate the high voltage required.

K. Clipping Amplifiers

The clipping amplifier chassis provides two limiting amplifier channels which are designed to give symmetrical clipping of the low-frequency input signals over a wide range of input voltages. Each amplifier consists of a three-stage, direct-coupled amplifier and a low-frequency, negative feed-back loop. The feed-back loop establishes the bias of the clipping threshold with respect to the input voltage so that, over the averaging time of the low-pass filter in the feed-back loop, the average width of the positive portion of the clipped output is equal to the average width of the negative portion. A potentiometer adjustment is provided to set the control point to maintain a ratio of the average positive and negative periods equal to unity. The schematic of the clipping amplifiers is shown in Fig. 30.

L. Control Panel

It was convenient to supply on the correlator rack a vacuum-tube voltmeter and negative bias supply which could be used for checking the operation

of the Deltic correlator. The schematic for this control panel is shown in Fig. 31. A pair of cathode followers form a high-impedance vacuum-tube voltmeter circuit which may be used for measuring the negative biases which are to be monitored. This voltmeter circuit may be connected to the desired circuit with the selector switch (SW_1). Four of the variable bias outputs are used to adjust the amplitudes of the pulses inserted at various points in the circuit. A push-button switch (SW_2) is inserted in the bias circuit for the clocking oscillator chassis. It serves to reset the control point of the automatic frequency control to the desired mode of operation, thus providing a vernier control on the relative phase of the clock pulse with respect to the recirculating pulses.

M. Power Supplies

The entire Deltic correlator was designed to operate from a 200-volt power supply, and a standard Lambda supply was obtained for this purpose. The entire correlator draws approximately 600 milliamperes exclusive of the recorder-motor driving amplifier.

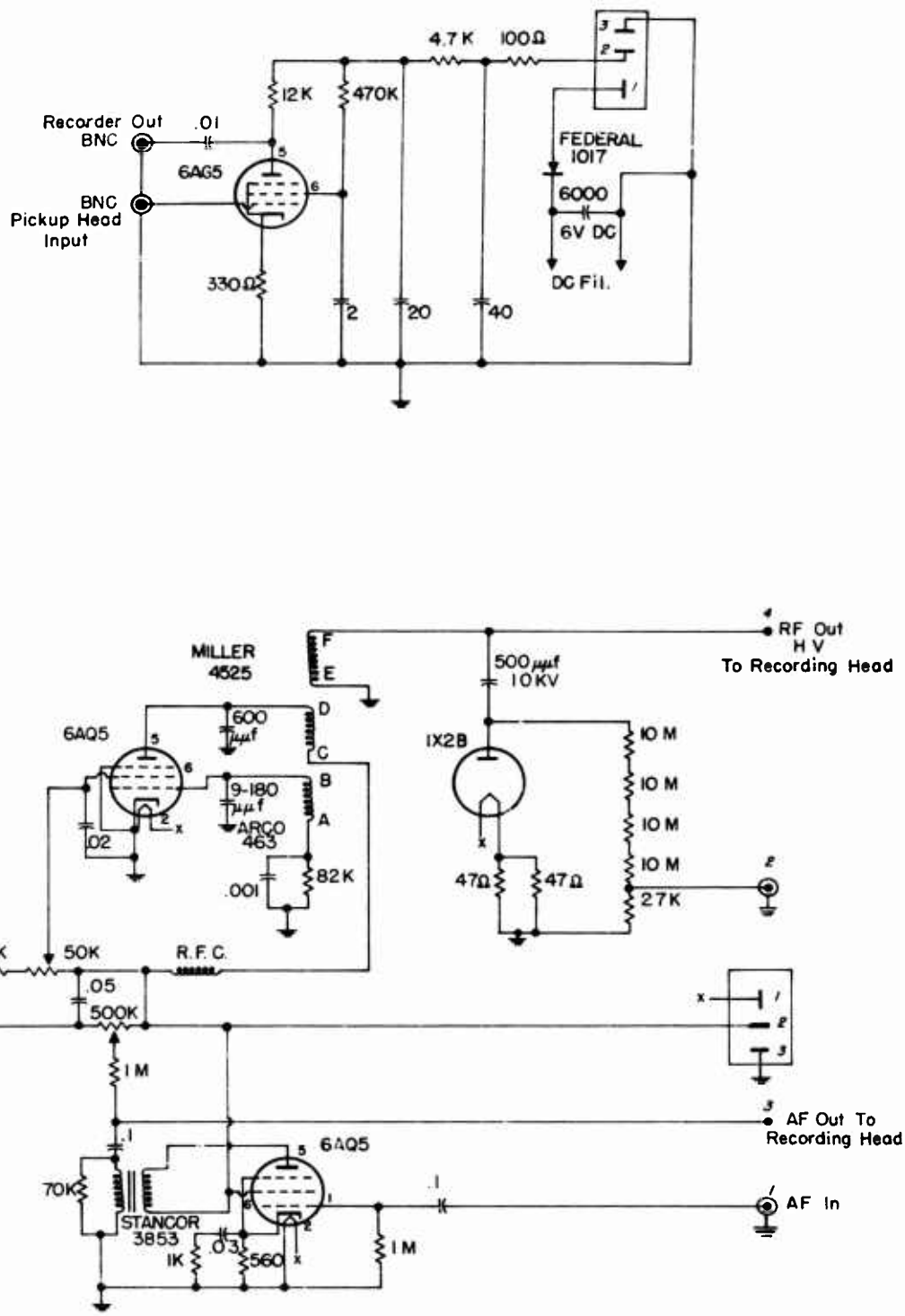


Fig. 29. Wiring diagram of the recording and playback amplifiers.

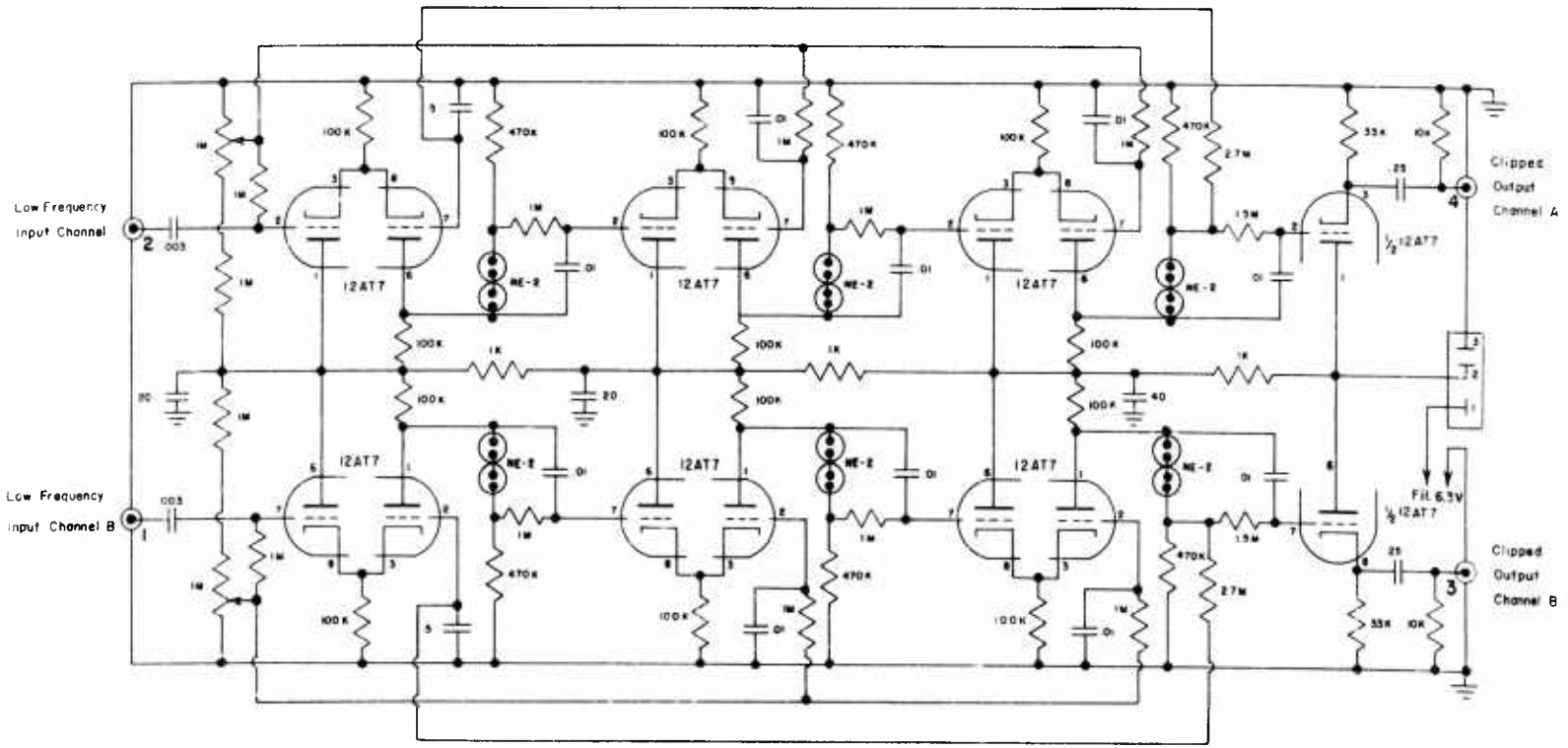
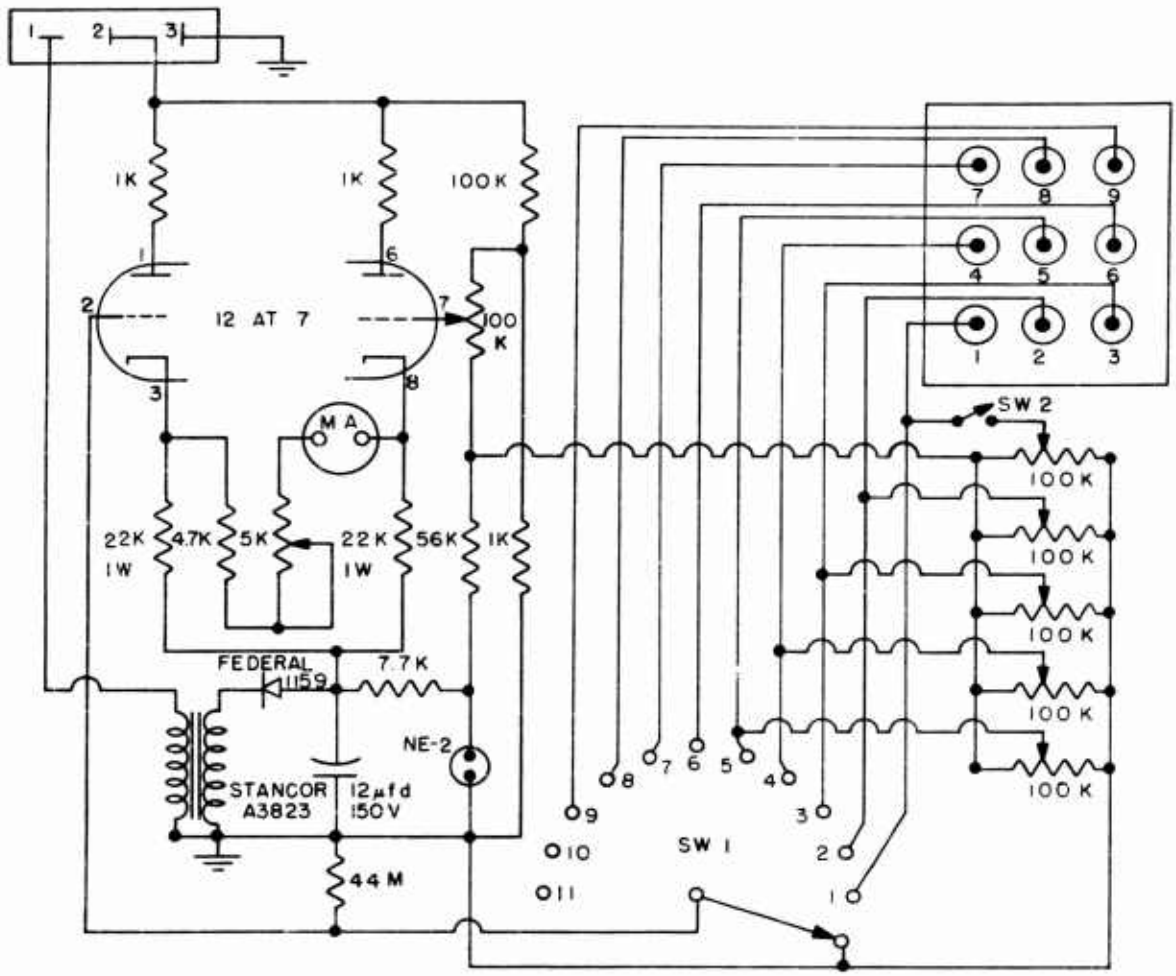


Fig. 30. Wiring diagram of the two-channel clipping amplifier.



1. AFC BIAS
2. CHANNEL A SAMPLING PULSE HEIGHT
3. CHANNEL B SAMPLING PULSE HEIGHT
4. TRANSFER PULSE HEIGHT
5. AUXILIARY BIAS OUTPUT
6. RF MONITOR VOLTAGE
7. AGC BIAS CHANNEL B
8. AGC BIAS STORAGE CHANNEL
9. AGC BIAS CHANNEL

Fig. 31. Wiring diagram of the control panel.

Chapter IV

NOTES OF DELTIC ALIGNMENT AND MAINTENANCE

One of the greatest problems which arose during the design and construction of the Harvard Deltic correlator was that of developing suitable test procedures which would indicate the operation of each of the various components of the Deltic before and after assembly. Although the testing procedures in themselves may not be unique, the aggregate of the various procedures used should serve to point out some of the difficulties which are present in the Deltic circuitry and as such have its place in the report. This section on testing procedures will, of course, be most useful to those actually operating the Deltic or those considering construction or possible redesign of such a device. The procedures will be listed in the order required for the initial set-up of such a Deltic correlator.

A. Cable Connections and Inter-Chassis Wiring

Figure 32 is a schematic of a complete Deltic, showing the interconnections between the various chassis. The plug numbering on this schematic corresponds to the numbers on the individual schematics which have been presented previously. The layout of the chassis blocks on the schematic corresponds as closely as possible to the physical location of the chassis as viewed from the rear of the relay rack.

B. Band-Pass Amplifiers and Delay-Line Coupling Networks

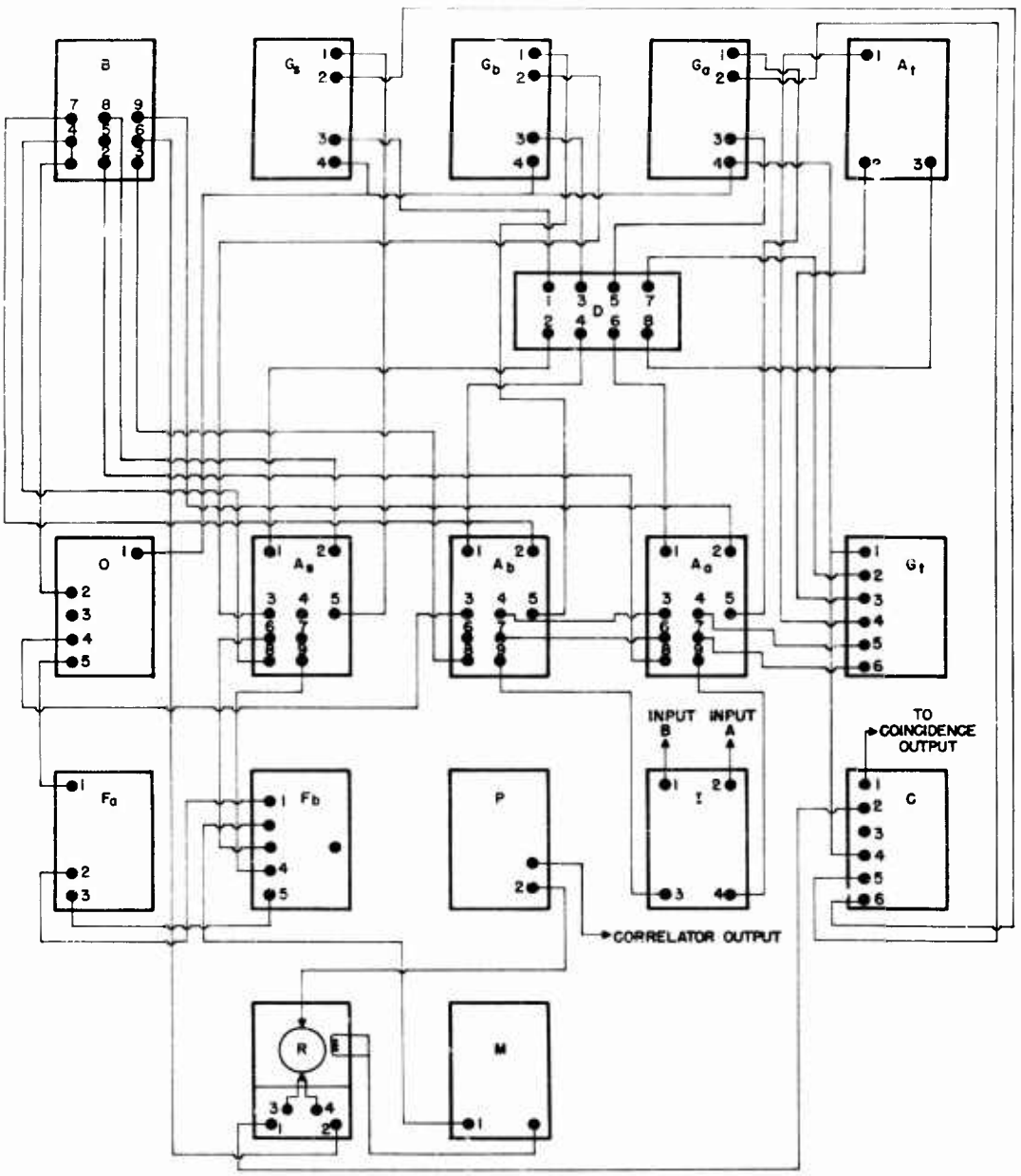
The initial alignment of the band-pass amplifiers is carried out with the use of a sweep frequency generator and a crystal diode detector probe. The sweep frequency generator used should have a sweep width of at least 10 Mc/s and cover the range from 20 to 40 Mc/s. After initial construction, the plate tuning coils are first checked for resonant frequency with the tubes in place and power on. This is accomplished by disconnecting the damping resistors (R_1) in the grid circuits and coupling into and out of each individual coupling network from the preceeding and succeeding amplifier tubes respectively. As is conventionally the case, the alignment is started from the output end of the band-pass amplifier (V_5) and carried through step by step to

the first coupling network (V_1). Each plate circuit inductance (L_1) is trimmed to resonate at the same frequency. In the present case, this was 33 Mc/s. Since the input capacity of the 6AK5 tubes is a function of the bias voltage, it is necessary to establish a nominal bias of approximately -1 volt on the AGC bus during this tuning operation. It may also be necessary to remove some of the other tubes in the amplifier to prevent oscillation because of the high gain of the amplifier when the damping resistors on the individual stages are disconnected.

After each individual stage has been peaked to the center frequency, the damping resistors (R_1) are connected to the grid terminals once more, and the alignment procedure is repeated. This time the series resonant damping circuit is tuned to obtain the desired, flat-topped response curve. Again the alignment procedure starts from the output end of the amplifier and proceeds back to the input. In this procedure, it is not necessary to shift the detector probe to each succeeding stage in the amplifier; it may remain at the output stage while the input signal is moved stage by stage toward the input end of the amplifier.

Capacitive divider networks have been installed permanently on each stage so that a detector probe may be coupled to each interstage network without seriously disturbing the tuning of the network. These divider networks consist of a 0.5 μμfd condenser in series with the shunt capacity of a panal mounting pin jack which is approximately 2 μμfd. When this shunt capacity is effectively shorted to ground by the detector probe, the total series divider capacity changes from 0.4 μμfd to 0.5 μμfd, a total change of 0.1 μμfd, which may be considered negligible in its detuning effect on the circuit.

After the interstage coupling networks of the band-pass amplifier are aligned, the delay line is connected to the amplifier and the sweep signal generator is connected to the input of the delay line through a 90-ohm to 10-ohm resistive attenuator pad to terminate the end of the cable suitably. The output termination of the delay line is then aligned in a manner similar to that for the interstage coupling networks. The damping resistor (R_2) is first disconnected and the parallel resonant inductance is tuned to the 33 Mc/s center frequency. Then the damping resistor is reconnected, and the series



B = Control Panel, Fig. 31.
G_s = Storage Channel Reclocking Gate, Fig. 12.
G_b = Channel B, Reclocking Gate, Fig. 12.
G_a = Channel A, Reclocking Gate, Fig 12.
A_t = Timing Channel, 30 Mc/s Amplifier, Fig. 10.
O = 10 MC Clock Oscillator, Fig. 18.
A_s = Storage Channel, 30 Mc/s Amplifier, Fig. 10.

A_b = Channel B, 30 Mc/s Amplifier, Fig. 10.
A_a = Channel A, 30 Mc/s Amplifier, Fig. 10.
G_t = Timing Channel, Reclocking Gate, Fig. 15.
F_a = 32:1 Frequency Divider, Fig. 20.
F_b = 10:1 Frequency Divider, Fig. 22.
P = Playback Amplifier, Fig. 29.
I = Two-Channel Clipping Amplifier, Fig. 30

C = Coincidence Circuit, Fig. 24.
R = Recording Amplifier, Fig. 29.
M = Motor Amplifier

Fig. 32. Wiring diagram of the inter-chassis cable connections.

resonant inductance is tuned for a flat-topped response. During this operation, the gain of the band-pass amplifier is used to build the signal up to the level necessary for the detector probe, which again is located at the output of the band-pass amplifier.

After the output network of the delay line is aligned, the input to the delay line is connected to the reclocking gate chassis, the sweep signal fed in through the capacitive divider network provided, and the alignment procedure carried out on the input termination network. During this alignment, it is convenient to remove the power from the reclocking gate chassis so that no spurious signals will be present in the 6AS6 reclocking gate tube (V_2). Again the parallel resonant tank circuit is tuned to 33 Mc/s with the series damping circuit disconnected, the series damping circuit is then connected and the overall response is tuned for a flat-top characteristic.

This alignment procedure is repeated for all four of the band-pass amplifiers in the Deltic correlator The final adjustments of the band-pass amplifier-delay line combinations may be carried out after a pulse train has been set up in the recirculation line, and the shape of the output pulses is observed on the cathode-ray oscillograph.

C. Timing-Channel Gating Chassis and Clocking Oscillator

After the band-pass amplifiers have been aligned, it is possible to proceed with the timing-channel gating circuits. Some convenient length of delay cable is chosen for this initial adjustment to interconnect the timing-channel gating chassis with the band-pass amplifier chassis for this channel. It is wise to choose the delay line at least one digit longer than the minimum length required for the interconnection of these chassis so that the shorter delay loops of the sampling channels may be connected with an adequate length of cable. After an arbitrary length of cable has been selected, it is connected between the input of the timing-channel gating chassis and the + gate output of the Tektronix scope, with a 2,000-ohm terminating resistor inserted in series at the output terminal of the scope. A low-capacity probe is connected at the input of the delay cable, and the reflected pulse from the input termination in the timing-channel gating chassis is observed on the oscilloscope display. The inductances in the input terminating networks

(L_1, L_2) are then adjusted to give a minimum amplitude reflection from the delay cable.

This same procedure is used in the other gating chassis in the sampling channels and storage channel. In the case of the timing-channel gating chassis, an approximate termination giving reasonably reflection-free operation is satisfactory, but the termination is much more critical in the case of the other channels. After this input termination has been matched to the cable, the input is left open or shorted, as desired, and the free running period of the multivibrator is set to approximately 40 μsec. The loop is then completed by connecting the output terminal of the timing-channel gating chassis to the input of the delay line, the delay line output to the input of the band-pass amplifier, and finally the band-pass amplifiers to the timing-channel gating chassis with the section of delay cable.

The automatic frequency control voltage of the clock oscillator chassis is set at 2.0 volts by shorting out the push button switch on the control panel and adjusting the bias control potentiometer. The tuning condenser (C_1) on the clocking oscillator chassis is then tuned to 10 Mc/s by comparison with some standard reference oscillator. After the clock oscillator is set to a 10 Mc/s frequency, the clock-pulse driver amplifiers may be aligned in all of the chassis. This is accomplished by observing the waveform at the capacitive divider on the input of the 6AS6 reclocking gates while the two inductances in the plate circuits are tuned. In this tuning process, the adjustment of the two coils is not independent; one circuit couples into the other in such a way that successive approximations must be used for the final adjustment. The low-frequency coil, which is one shunted with the 100 μμfd condenser, is first tuned to resonate at 10 Mc/s, and then the series plate coil is tuned to resonate at 30. By suitable tuning, a waveform such as that shown in Fig. 14 can be obtained.

With the clock oscillator operating at a 10 Mc/s rate, the timing-channel multivibrator should now lock in at the period of the recirculation loop. In the initial design of the timing-channel gating circuit, it was necessary to trim the length of the delay cable used as the pulse-shaping network in the output of the multivibrator plate, for the reasons outlined in the previous chapter.

The relative phase between the clock oscillator and the sampling pulse must be adjusted so that, when the detector tube is operating in the center of its control range, the leading edge of the pulse from the multivibrator plate will fall half-way between two clock pulses. This will give the greatest stability in operation and permit the greatest tolerances for small phase errors in the recirculation loop.

The final trimming of the band-pass amplifiers of this channel may be accomplished by observing the shape of the returned pair of pulses coming into the timing-channel gating chassis, and adjusting the shunt peaking coil on the output of the reclocking gate to equalize the relative amplitudes of the two pulses in the pair. After these procedures have been followed, the AFC control loop may be closed and the oscillator should lock into one of the normal modes of the line.

D. Frequency-Divider Chassis

The frequency-divider chassis may now be connected as indicated in the schematic of Fig. 32. The waveforms of Figs. 21 and 23 may be used as a guide to check the operation of the two chassis if any difficulty is experienced in their operation. The trigger output of the 10:1 divider chassis may be used to synchronize the delaying sweep of the oscilloscope to the period of the correlation sweep. This will provide a convenient time base for observing the operation of the sampling and storage channels of the Deltic

E. Sampling Channel

The first step in the alignment of the sampling channel is to select an arbitrary length of delay cable suitable for interconnecting the reclocking gate and the band-pass amplifier. The adjustment of the cable termination is checked as in the case of the timing-channel gating chassis by inserting the + gate signal from the Tektronix through a matching resistor to the free end of the cable and observing the pulses reflected from the chassis termination. After the termination has been adjusted and the response of the driver amplifier plate tuned for an optimum overshoot of 5 per cent, the cable may be connected to the band-pass amplifier chassis.

The proper length for this interconnecting delay cable may now be

determined by inserting the sampling pulse at the sampling pulse input to the new information gate on the band-pass amplifier chassis, leaving the erasing pulse disconnected for the time being, and observing the phase of the pulse when it reaches the suppressor grid of the 6AS6 reclocking gate (V_2) in the reclocking-gate chassis. The time error between the center of the pulse transmitted to the suppressor grid of the reclocking gate and the clock pulse may be read directly from the oscilloscope, and the length of cable may then be trimmed to set this phase error equal to zero. It is advisable to start with cable several inches longer than the minimum length which will fit between the chassis, and then to trim them down until they correspond to the nearest correct multiple of the sampling pulse interval.

The easiest way to observe this phase error is to insert phase markers derived from the clock pulse in the Z-axis of the oscilloscope. This was accomplished by using a New London Instrument Co. broadband pulse amplifier and a section of 1,000-ohm de' .y cable which was trimmed to adjust for the difference of delay between the oscilloscope deflection amplifiers and the pulse amplifier used for these timing pulses. The timing of these pulses was adjusted so that the bright spot on the screen occurred at the peak of the clocking pulses as observed in the oscilloscope.

After the interconnecting cable length has been adjusted, the output of the reclocking gate chassis is connected to the input of one of the delay lines in the delay line package; the output of this delay line is connected to the band-pass amplifier of an adjacent channel, to prevent recirculation in the loops. It is now possible to observe the arrival of the transmitted pulse at the output of this band-pass amplifier and to compare it at this point with the phase of the incoming sampling pulse. The time difference between the transmitted pulse and the sampling pulse must be adjusted to one digit interval (0.1 μsec). This adjustment is carried out by changing the length of the cable connecting the band-pass amplifier and the reclocking gate chassis of the previously aligned timing channel. Care should be taken in making this measurement and adjustment to insure that the clock oscillator is operating in the correct mode, that the clock-pulse amplifiers are properly tuned, and that the multivibrator period is set to generate a symmetrical square wave, since errors in these circuits may cause a relative phase error

of as much as two or three tenths of a digit interval.

During these tests, where only a single pulse per recirculation period is introduced into the band-pass amplifiers, it is necessary to supply an auxiliary bias to the AGC bus. This bias may be supplied by moving the monitoring connections to the auxiliary bias connector on the monitor control panel (No. 5). The bias voltage is adjusted so that a normal size pulse appears at the output of the band-pass amplifier.

The alignment process outlined above should be repeated for the second sampling channel. Once the terminating networks and the lengths of the interconnecting delay cables have been adjusted, the sampling channels may be connected together into recirculation loops: that is, the output of the reclocking chassis of one chassis pair may be connected to one of the delay lines, and the output of this delay line connected to the band-pass amplifier of the same pair. It is now necessary to insert the erasing pulse into the correct input on the band-pass amplifier chassis so that the sampling process may be carried out. With the loop complete, a low-frequency square wave input may be introduced into the low-frequency gate input on the band-pass amplifier chassis, and the final alignment of the band-pass amplifier tuning can be adjusted by observing the shape of the train of pulses derived from the sampling of this square wave input.

If these pulses or pulse trains are to be observed as a stationary pattern on the oscilloscope, it is necessary to lock the oscilloscope to some sub-multiple of the sampling-pulse period or loop recirculation period. This may be accomplished by connecting the sampling pulse to the main sweep trigger input and triggering the delaying sweep with the synchronizing pulse from the 10:1 divider.

The delayed trigger may then be used to select one recirculation sweep or fraction thereof out of the correlation sweep. A more stable display is obtained by inserting the sampling pulse into the main-sweep trigger instead of using only the delaying trigger to initiate the main sweep. In order to obtain a stable display, the trigger threshold must be adjusted so as to synchronize the start of the main sweep with the occurrence of the sampling pulse.

By setting the square wave generator to a sub-multiple of the sampling pulse frequency in the neighborhood of 1 kc/s, one can now obtain a stationary set of pulse groups on the face of the cathode-ray oscillograph as shown in Fig. 33. It may be necessary to adjust the level control of the band-pass amplifier AGC circuit to obtain an optimum recirculation storage which is characterized by stably maintaining these pulse groups over the entire recirculation period. It may also be necessary to adjust the height of the sampling pulse by use of the appropriate bias control on the control panel in order to avoid introducing extraneous pulses into the line or to avoid pulse levels too low for positive operation of the gate.

The final trimming of the band-pass amplifier and delay-line terminating networks is accomplished by tuning the output network of the reclocking gate to obtain amplitudes of the leading and trailing pulses in the recirculating pulse group equal to the other pulses in the group.

F. Storage Channel

The alignment of the storage channel proceeds in a manner similar to that for the other two recirculation channels. The interconnecting cable for the band-pass amplifier and reclocking gate chassis of the storage channel may be cut to length initially by measuring a length sufficient to give one digit delay, 0.1 μsec, more delay than the cable connecting the band-pass amplifier and reclocking gate chassis of the sampling channel. The terminating network and the peaking coil for the driver amplifier in the re-clocking-gate chassis are adjusted as outlined in the previous procedures.

The delay cable connecting the output of one of the sampling channels to the storage-channel new-information gate is cut to the length required to phase the arrival of the pulse train from the sampling channel to be synchronous with the clock pulses at the suppressor of the reclocking gate. While carrying out these adjustments, it is advisable to supply a bias to the AGC bus of the band-pass amplifier high enough to reduce the gain below the re-circulation level.

After adjustment of this interconnecting cable is completed, the AGC bus may be restored to normal operation, and the storage channel will re-circulate pulses in a stable manner. It is necessary to adjust the amplitude

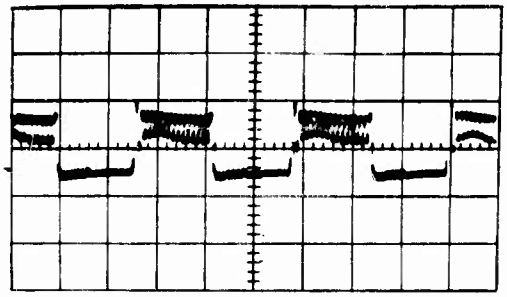
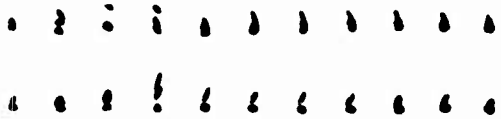


Fig. 33. Recirculating pulse train (1 kc low-frequency input).



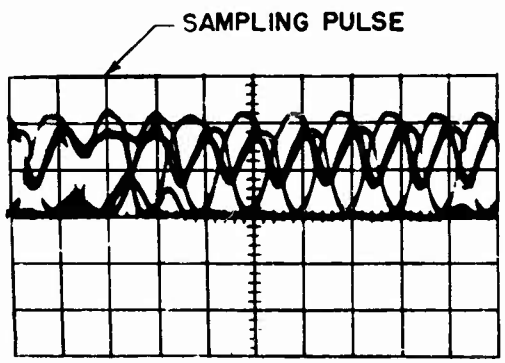


Fig. 34. Composite picture of recirculating pulses.

of the bias for the transfer pulse so that the level of the pulse height of the incoming pulse train is equal to the height of the pulses which are recirculated. This may be done by observing the entire 9.8 ms period of the line on the oscilloscope, using the 9.8 ms trigger output from the 10:1 divider chassis to trigger the delaying sweep of the Tektronix oscilloscope. The portion of the pulse train corresponding to the transfer pulse interval may be expanded with the main sweep and examined in more detail to determine whether or not the information which is being inserted into the line is suitably reproduced by the pulse train which is recirculated in the stable manner.

One of the easiest ways of checking the operation of any of the recirculation channels is by observing the composite picture of leading and trailing pulses superimposed upon the normal pulses in the line, which display can be obtained by triggering the oscilloscope on the main sweep from the sampling pulse, and observing the signal on the suppressor grid of the reclocking gate. Such a trace is shown in Fig. 34. The position of the Z-axis clock-pulse markers can be observed on each of the types of pulses which are recirculating in the loop, and the phasing for optimum stability can be determined from this type of trace. With reduced intensity on the screen, the clock-pulse markers are distributed in two groups as shown at the bottom of Fig. 34. The blank space between these two groups is an indication of the stability of operation or the stability of recirculation in the line. This vacant space should occur at a voltage range which is centered about the center of the saturation curve for the reclocking gate shown in Fig. 13. The correct amplitude for the sampling pulse may also be determined from this display, again checking for optimum stability in the position of the clock-pulse markers. This type of test is not restrcited to the use of a sinusoidal or periodic signal at the input of the sampling channels; it is equally valuable in use with a random input signal such as thermal noise. The space between the two groups of marker pulses indicates the degree of stability with which the information is recirculated in the line.

G. Coincidence Chassis

The remaining necessary phase alignment is that of cutting the cables between the sampling channel and the coincidence chassis, and between the

storage channel and the coincidence chassis. These two cables must be cut to different lengths to correct for the time delays which are introduced in passing from the data insertion gate on one of the recirculation channels to the output gate. This difference in time delay must be made equal to the sum of the delays of the interconnecting cable between the sampling channel and the storage channel,the interconnecting cable between the band-pass amplifier and the reclocking chassis of the storage channel, and the time delay offset which is desired to place the zero of the correlation delay in the correlation sweep. This total delay amounts to about 10 digits or one μsec of delay time, corresponding roughly to an additional 10 feet of cable.

The phasing of each length of cable must be carried out individually. The power is removed from the reclocking gate chassis to which the end of the cable not under consideration is connected, so that the propagation time in the cable of interest may be observed without interference. The arrival of the pulse train at the input to the coincidence chassis may then be observed on the oscilloscope and the length of cable adjusted so that the phasing of the pulse train at this point with respect to the clock pulses, is optimized as outlined previously. With this cable cut to the proper length, the procedure may be inverted, and the process repeated for the other cable

After the two cables have been individually cut to the proper lengths, they may be reconnected to their respective chassis and the signal at the input to the coincidence chassis may again be observed on the oscilloscope. This signal will now be a three-level signal with three distributions of marker pulses if the composite display outlined previously is used If the cable terminations are satisfactory and the pulse train shape from each of the chassis is of the correct magnitude, the blank spaces between the three groups of pulses should be centered about the two thresholds of the coincidence circuit, as shown in Fig. 26b. If these voltage regions do not coincide, they can be adjusted by changing the divider network of the coincidence circuit or by changing the amplitude of the pulse train, this being accomplished by adjusting the value of the divider circuit in the plates of the driver amplifier on the reclocking-gate chassis.

When these correct voltage ranges have been established, the inverter stage should be checked for balance by displaying the curve of Fig. 26 b on

the oscilloscope. This curve is displayed by simultaneously applying a sine-wave signal of approximately 300 c/s both to the X-axis of the oscilloscope, after having calibrated the X-axis gain, and to the input of the coincidence circuit with both of the delay cables removed. The vertical amplifier is connected to the output of the correlator. The return step of the inverter stage can be balanced by trimming the resistances in the appropriate 6AS6 plate circuit (V_1 or V_2) to obtain a reasonably flat base line.

At this stage of the alignment procedure, it should be possible to obtain the correlation of a periodic wave by introducing a sine wave into both inputs of the clipper amplifiers and observing the output of the coincidence chassis on the oscilloscope, triggering the sweep of the oscilloscope from the trigger output of the 10:1 divider chassis, which has a period corresponding to the correlator sweep. The output should be a roof-top wave, the individual sampling periods showing up as steps or breaks in this triangular wave, particularly as the frequency of the input is increased. The peak-to-peak amplitude of this correlation output should remain constant up to the maximum operating frequency and above. Sample correlation sweeps are shown in Fig. 35.

There will be particular frequencies at which the correlator will drop out of operation. At the low frequency (100 c/s) there will be a certain amount of flutter introduced because of the finite length of sample which will contain only a few cycles of information, while at the high-frequency end (above 5 kc/s) there will be a peaked frequency pattern appearing as shown in Fig. 36, which is caused by the beating or interference between the 30 kc/s sampling frequency and the input frequency. This peaking will be most noticeable when the input frequency approaches a submultiple of the 30 kc/s sampling frequency.

H. Integrating Drum

The operation of the integrating drum is simple in comparison with the operation of the previous sections of the Deltic. There are three adjustments on the dielectric recorder which one needs to be concerned with: (1) the RF voltage adjustment on the recording head, (2) the slit opening of the recording head and (3) the DC bias of the recording electrode.

The RF voltage should be set at a level sufficient to give a stable discharge; this will fall between 2,000 and 2,500 V rms. For very long time constants, it may be wise to set this at the lowest level possible in order to increase the effective impedance of the recording head, while for short integration times, a higher RF level may give rise to a more noise-free and more stable operation of the recording head.

The slit opening is adjusted to give the suitable time constants desired and can be controlled over a range of a few tenths of a mil to approximately 30 mils gap, a variation which will carry the integration time from approximately 100 seconds to 0.1 second.

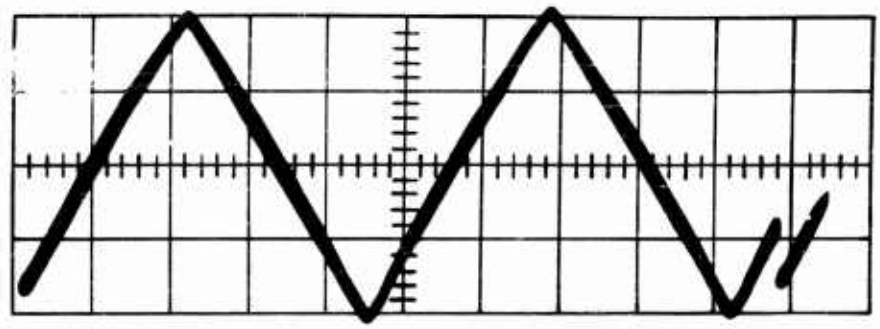
The zero-signal potential of the dielectric surface is adjusted to be near ground potential by means of a DC-balance potentiometer on the recording chassis. This minimizes the effects of surface irregularities and drum eccentricities in generating spurious signals on the pickup probe.

The amplitude of the motor drive for the dielectric recorder is set to give an overall voltage of approximately 170 volts with the drum running synchronously. The adjustment of this output is rather critical; if the amplitude is too low, there will not be sufficient power to pull the drum into synchronism, while if the gain of the amplifier is set too high, the distortion of the signal will prevent the drum from locking in truly synchronously and there will be a residual slip which will degrade the signal stored on the drum.

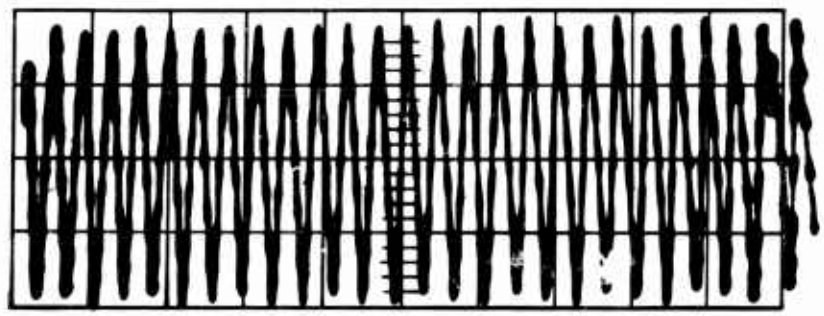
I. Clipping Amplifiers

The two clipping amplifiers must be adjusted to give symmetrical clipping if one is to obtain a true correlation function. Asymmetrical clipping will become evident in the correlation of a sine-wave input by the flattening of either the upper or the lower peaks of the triangular waveforms of the correlation function.

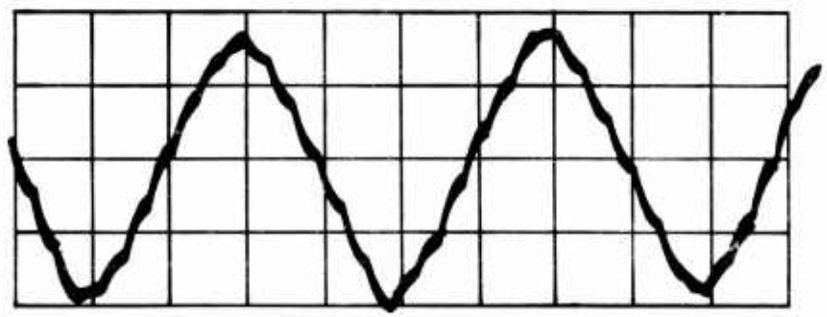
The clipping symmetry is set by inserting a sine-wave signal into the input of the clipping amplifiers, and observing the average DC voltage of the output. An easy way to adjust this is to set the oscilloscope on AC input, center the trace vertically on the screen for zero signal in, and then, with the scope connected to the clipper output, adjust the clipping threshold control to make the positive and negative excursions of the clipped signal symmetric about the center line.



200 C/S



4 KC/S



4 KC/S
EXPANDED SWEEP

Fig. 35. Correlator output for a 200 cycle sine-wave input and a 4 kc input.

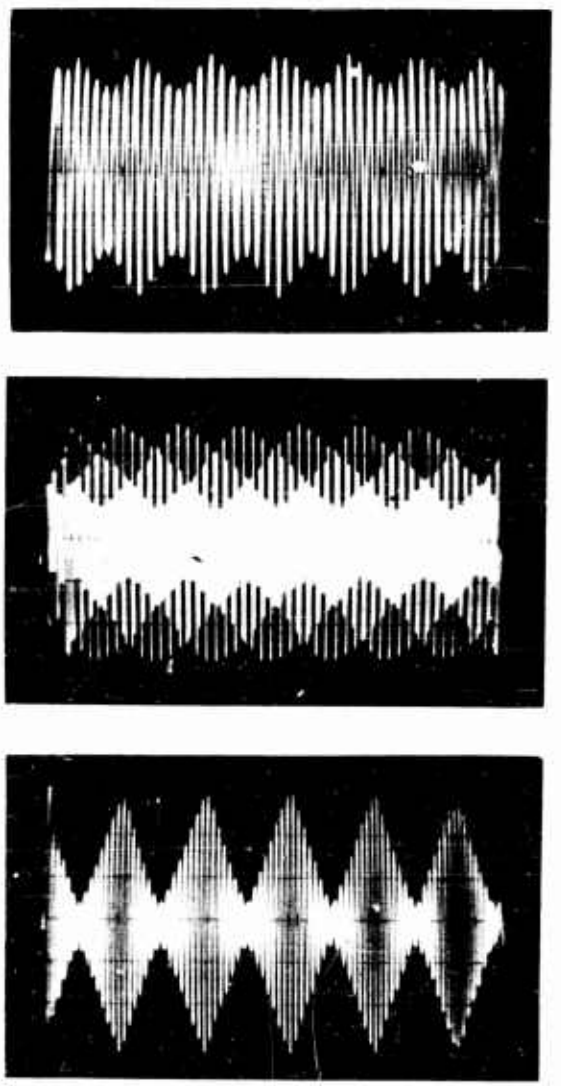


Fig. 36. Interference pattern appearing in high frequency sine-wave correlation output.

Chapter V

DELTIC CORRELATOR PERFORMANCE

After completion of the construction of the Deltic correlator, a series of tests was carried out to evaluate its performance. These tests were by no means comprehensive or exhaustive, but did suffice to demonstrate the effectiveness of the device. The numerical results obtained are the first step in evaluating the effectiveness of the device for signal-to-noise-ratio enhancement by the use of correlation techniques. One of the most valuable aspects of the Deltic correlator arises from the simultaneous display of the correlation function. The advantage of this type of display over the slow point-by-point plot obtained with conventional correlators cannot be measured quantitatively. It became evident that the ability to observe changes in correlation function with the variation of different parameters of the input signals leads one rapidly to an intuitive understanding of the correlation technique as a tool in data processing, an understanding which is essential to the effective application of the technique, but is most difficult to obtain by any other means.

The numerical results obtained from these tests are sufficient to answer some of the initial questions which were raised concerning the utility of the Deltic correlator for signal processing.

There were two points in question regarding the operation of a Deltic correlator, one being the loss of information which could be expected from the combined sampling and clipping process; the other, the effectiveness of the dielectric recorder integration. The results for clipping alone have been fairly well covered theoretically in the references previously mentioned by Faran and Hills and others. The effect of sampling alone, retaining the full amplitude information of the samples, has been covered theoretically by Shannon [3], who has shown that a loss of information due to finite-time sampling would not occur provided the sampling rate was higher than twice the highest frequency in the signal that was sampled. The question arises

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3. B. M. Oliver, J. R. Pierce, and C. E. Shannon, "The Philosophy of PCM," Proc. Inst. Radio Engrs. 36, 1324-1331 (November 1948).

as to whether the highest frequency which need be considered in the combined case is the frequency of the incoming signal before clipping or the frequency of the higher distortion components introduced by the non-linear clipping process. There is no effective theoretical treatment for this combined case, although Bennett [4], has treated the problem of amplitude quantization and time quantization of signals for a minimum of eight amplitude quantum levels as compared to the two levels (+,-) occurring in this total clipping process. Private communications with others concerned with this problem of total clipping and time sampling have indicated that a sampling rate of three times the highest frequency does not appear to result in a significant loss of information. This is a rule-of-thumb approach to the problem; the ratio of 3:1 has been gained from practical qualitative observations of the effect of the sampling frequency on the signal-to-noise ratio.

In an attempt to establish the optimum sampling rate more definitely, a series of measurements was carried out on the Deltic correlator operating as an autocorrelator (i.e., the same input to both channels). A true rms detector was used to measure the power output of the correlator as a function of the frequency of a sinusoidal input signal. The detector consisted of an rf thermocouple-type milliammeter which was placed in the output of a McIntosh amplifier. A calibrated attenuator was inserted in the input circuit of the McIntosh amplifier between the amplifier and the correlator output, and this attenuator was adjusted to maintain a constant output on the rf thermocouple milliammeter as the frequency was varied. The relative frequency-power response of the correlator as determined by this attenuator setting is plotted in Fig. 37 and shows the loss in power which is to be expected as one approaches the usable high-frequency band limit of the correlator. It can be seen that below 10 kc, which is one third of the 30 kc sampling rate, the curve rises very rapidly to the reference level, the amplifier response of the output stage of the correlator. If a rectangular low-pass spectrum is assumed, the data of Fig. 37 will yield the total power-loss curve shown in Fig. 38 where the power loss of the output

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4. W. R. Bennett, "Spectra of Quantized Signals," Bell Syst. Tech. J. 27, 446-472 (1948).

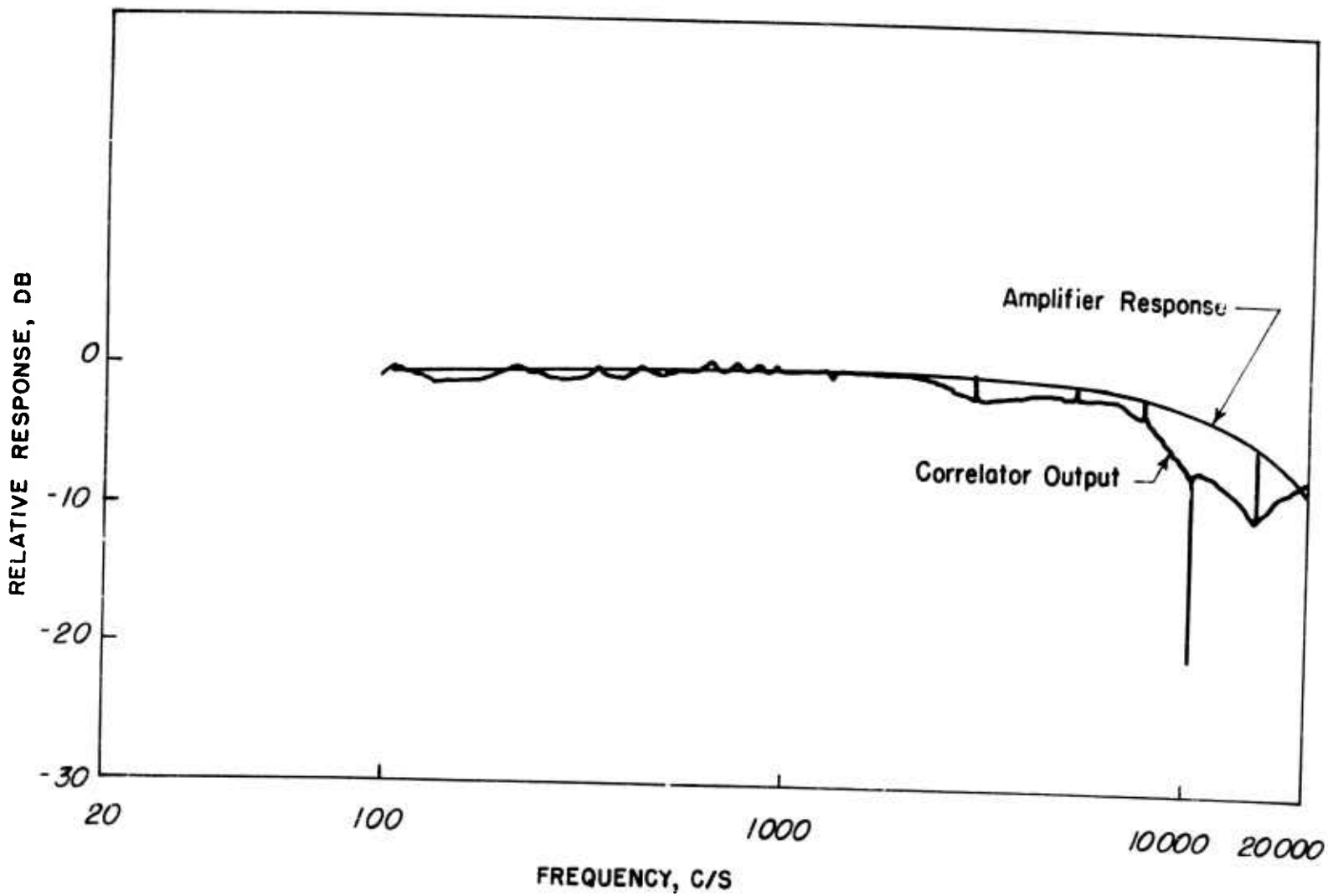

Fig. 37. Frequency-power response of the Deltic correlator.

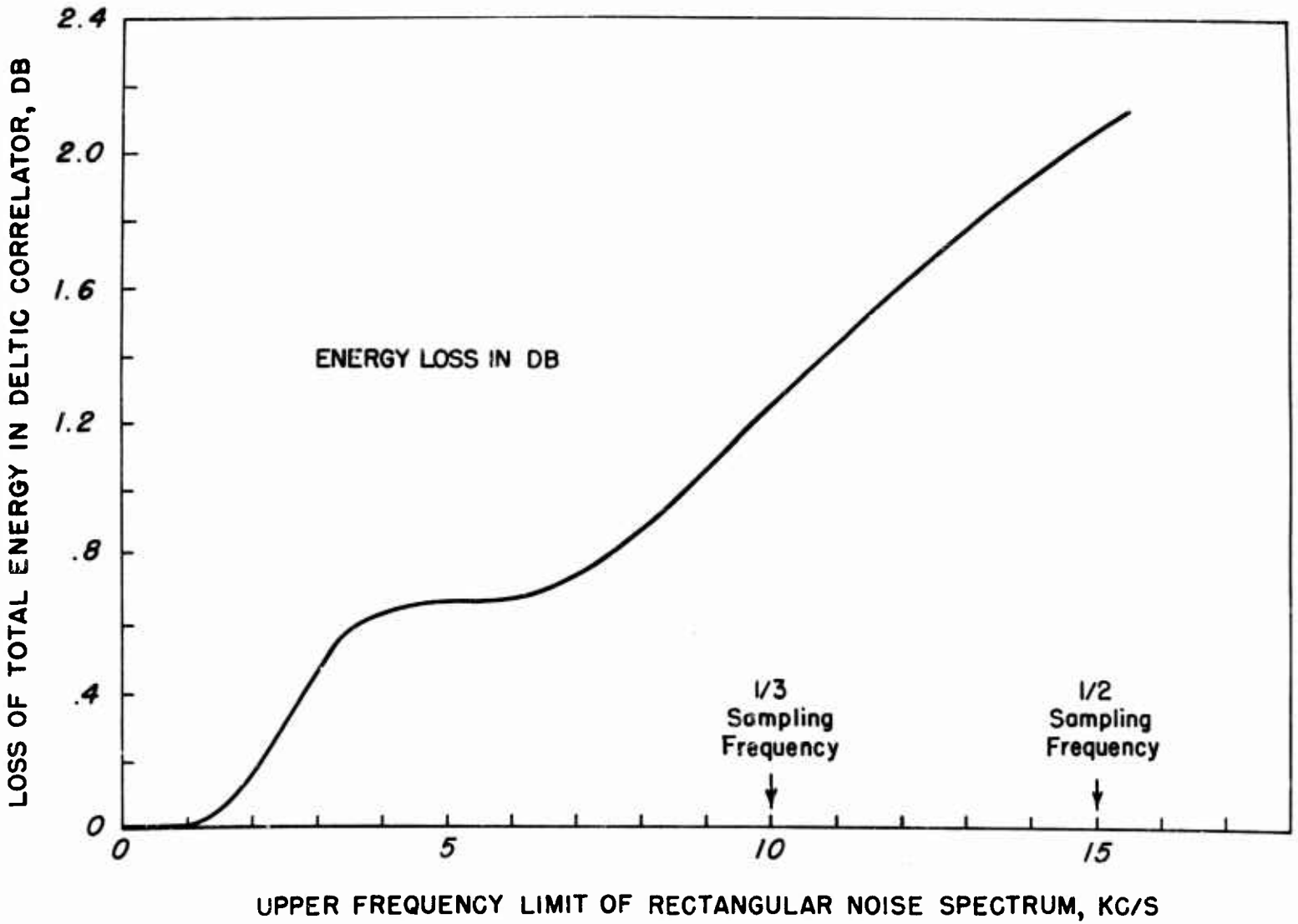

Fig. 38. Total power loss vs upper cutoff frequency of a rectangular input noise spectrum for the Deltic correlator.

correlation function in db is plotted against the upper cutoff frequency of a rectangular input noise spectrum. It can be seen that, for cutoff frequencies up to 10 kc/s, a loss of approximately 1 db or less may be expected; however, if a loss of 1/2 db is desired, the cutoff frequency must be carried down to approximately 3 kc, or 0.1 the sampling rate. These results for a rectangular spectrum would not necessarily represent the noise spectrum which might be present in any practical information channel; in such a case it would be necessary to weight the energy summation by the spectrum of the input signal, and a somewhat higher loss would be expected. Of course the complete answer to this question cannot be resolved until the variation of the background fluctuation noise as a function of frequency is also measured. It is hoped that in the future measurements, a figure for this fluctuation noise may be established.

It is interesting to note in the output curve of Fig. 37 that a number of point discontinuities appear in the curve. These discontinuities occur when the sampling rate is an exact multiple of the input frequency, so that the correlation pattern displayed on the oscilloscope builds up to a full amplitude signal and does not show the amplitude modulation which is present at frequencies other than this discrete frequency. The low-frequency end of the correlator response shows a cusped pattern which is brought about by the phase errors at the end of the correlation sweep. These peaks occur at multiples of the basic correlation sweep frequency of 100 cycles, and gradually disappear as more cycles are included in the correlation sweep, thus reducing the importance of the phase error at the end of the sweep.

Absolute measurements were also made on the fluctuation background noise for the correlator. A single-tuned-circuit noise spectrum was used to match the theoretical calculations that had been made by Faran and Hills [5] in their evaluation of polarity-coincidence correlators; a bandwidth of 300 c/s was used for all of the measurements, with center frequencies at 1850 c/s and 2450 c/s. The rms background fluctuation was measured by observing the signal level of the correlator output for two incoherent signals having identical noise spectra. An absolute calibration was obtained by measuring

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5. J. Faran and R. Hills, T.M. 27, 58-65, Harvard University Acoustics Research Laboratory.

the rms levels obtained with a sine wave centered in the spectrum of interest, and suitable corrections were made to refer the rms value of the background fluctuation to the peak value of the triangular correlation function which corresponds to a correlation of 1.0. The theoretical fluctuation noise for the integration time of the correlator, 9.45 ms, and a bandwidth of 300 c/s is - 15.8 db. The signal-to-noise measurements with the 2450 c/s filter gave a value of -15.0 db, and the measurements with the 1850 c/s filter gave a value of -14.90 db, resulting in errors of +0.8 db and +0.9 db respectively. The measurements were carried out at these lower frequencies so as to avoid the effects of the high-frequency sampling rate which are evident in Fig. 37. The expected error of the fluctuation measurement is somewhat less than $\pm$0.2 db; hence, the departure of 0.8 db from the theoretical figure may be significant. It is interesting to note that the measurements by Faran and Hills [op. cit] on the polarity-coincidence correlator showed the output of the correlator to be inferior to that of the multiplier-averager by 2 db with an expected error of $\pm$1.5 db. The 0.8 db measured with the Deltic correlator would correspond to a figure of 1.5 db when compared to a multiplier-averager according to theory. One may conclude that these departures from the theoretical results for the polarity-coincidence correlator are significant, therefore, and reflect a possible omission in the theory. It is also interesting to compare the relative accuracy of the background measurements as made with the Deltic (+0.2 db) and with the conventional correlator as performed by Faran and Hills [op. cit.] ($\pm$1.5 db). A factor of nearly 10 to 1 in expected accuracy reflects the great advantage to be gained by the 300:1 multiplication factor of the Deltic correlator. One reason for this increased accuracy is the fact that the spectrum of the correlation noise in the Deltic correlator corresponds to the spectrum of the input signal, both falling in the audio range where measuring equipment is readily available. With a correlator, the output spectrum of the fluctuation noise has the shape of the input noise, but is multiplied by the scanning rate as pointed out by Goff [6]. The scanning rate for the Deltic is equal to unity regardless of integration time. In contrast, a comparable conventional

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6. K W Goff, "Analog Electronic Correlator for Acoustic Measurements," J. Acoust. Soc. Am. 27 (no. 2), 223-236 (March 1955).

correlator would have a scanning rate ranging from $\sim 3 \times 10^{-3}$ for a 10 ms integration time to $\sim 3 \times 10^{-7}$ for a 100-second integration time. Thus, with a conventional correlator, the spectrum of the correlator noise for a 3 kc/s input spectrum falls in the frequency range of 10 c/s to 0.001 c/s, a region where accurate rms measurements are indeed difficult to carry out.

Similar fluctuation-background measurements were made to determine the effectiveness of the post-detection integration with the dielectric drum. In this case, relative fluctuation level measurements were made for various bandwidths of input noise signal, measurements being taken at both the input and the output of the dielectric recorder; the ratio between the two was compared with that expected for the measured time constant of the recording drum. The time constant of the drum was measured by recording the output of the recorder on a Bruel and Kjaer level-recorder and observing the slope of the decay curve when the input signal was removed. The time constant obtained from the slope of this decay curve was corrected by the ratio of the correlation sweep time to the stored signal length as indicated in the equations of Chapter 2. The values obtained are plotted in Fig. 39 where the measurements for the several noise bands are compared with the theoretical slope which would be expected. The theoretical lines shown do not necessarily represent the correct absolute values of background noise level, but are only correct in slope, and give the relative comparison of the additional effectiveness of the dielectric recorder post-detection integration time as compared to the finite-time integration of the Deltic correlator itself. The measurements were restricted to an integration time of 0.3 to 1.5 second because it was felt that the most significant measurements could be made in this range where the background recorder noise would be negligible, and where long period fluctuations in the recorder output level would not give rise to large uncertainties in the fluctuation level measurement. It can be seen that the additional integration time of the dielectric recorder gives rise to a reduction in the background fluctuation noise which very closely approximates the theoretical slope that would be expected.

In addition to the fluctuation noise measurements described above, some detection-threshold measurements were also made, using a sinusoidal signal

in a thermal noise background. The results of such an experiment are shown in Fig. 40. Here a set of displays of the correlation output from the dielectric drum are shown along with the filter response determining the input noise spectrum, and the build-up and decay curves for the dielectric recorder. In these tests, two independent noise generators were used; the outputs of these generators, after being fed through identical filters, were applied to the two channels of the Deltic correlator. A small 3 kc/s signal, whose amplitude could be accurately determined, was added to both of the input channels. As can be seen from the set of correlation curves of Fig. 40, which are run for a sequence of diminishing signal-to-noise ratios, the threshold detection lies in the neighborhood of -17 db for the particular parameters used in these tests. Without a large number of independent observer tests to establish a detection threshold, it is impossible to obtain more than a qualtitative indication. In this case an inaccuracy of perhaps $\pm$ 2 db might be expected on the -17 db threshold illustrated by the curves. If an output signal-to-noise ratio of unity is chosen as the detection threshold, the theoretical signal-to-noise ratio for threshold detection as referred to the input signal would be -21.5 db. This is computed on the basis of a rectangular band of input noise having a half-bandwidth of 1.7 kc, and a time constant of 1.8 seconds for the integrating drum. The results of this threshold test are in agreement with the previous results on the background fluctuation noise and the frequency response of the correlator. The previous results would modify the figure of -21.5 db by an amount of approximately 1.5 db due to the loss in energy resulting from the finite sampling time as illustrated by Fig. 37, and by another 0.8 db due to the increase in fluctuation noise which has been measured, giving an expected threshold of about -19 db. This is in qualitative agreement with the observation that the detection threshold lies between -16 and -18 db as shown by the curves of Fig. 40. Further measurements of a more quantitative nature are necessary to establish this threshold more definitely.

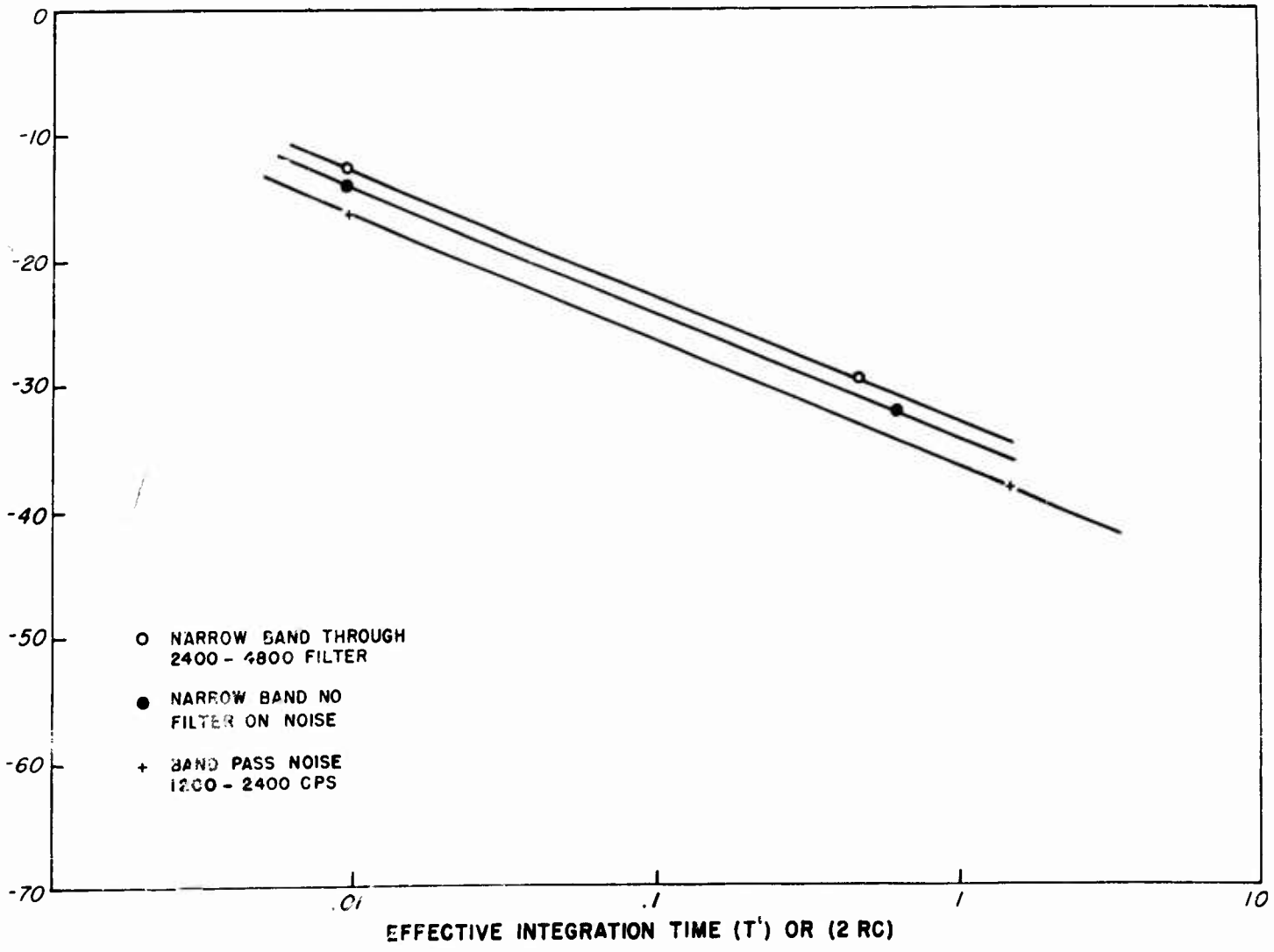

Fig. 39. Correlator output fluctuation noise vs integration time.

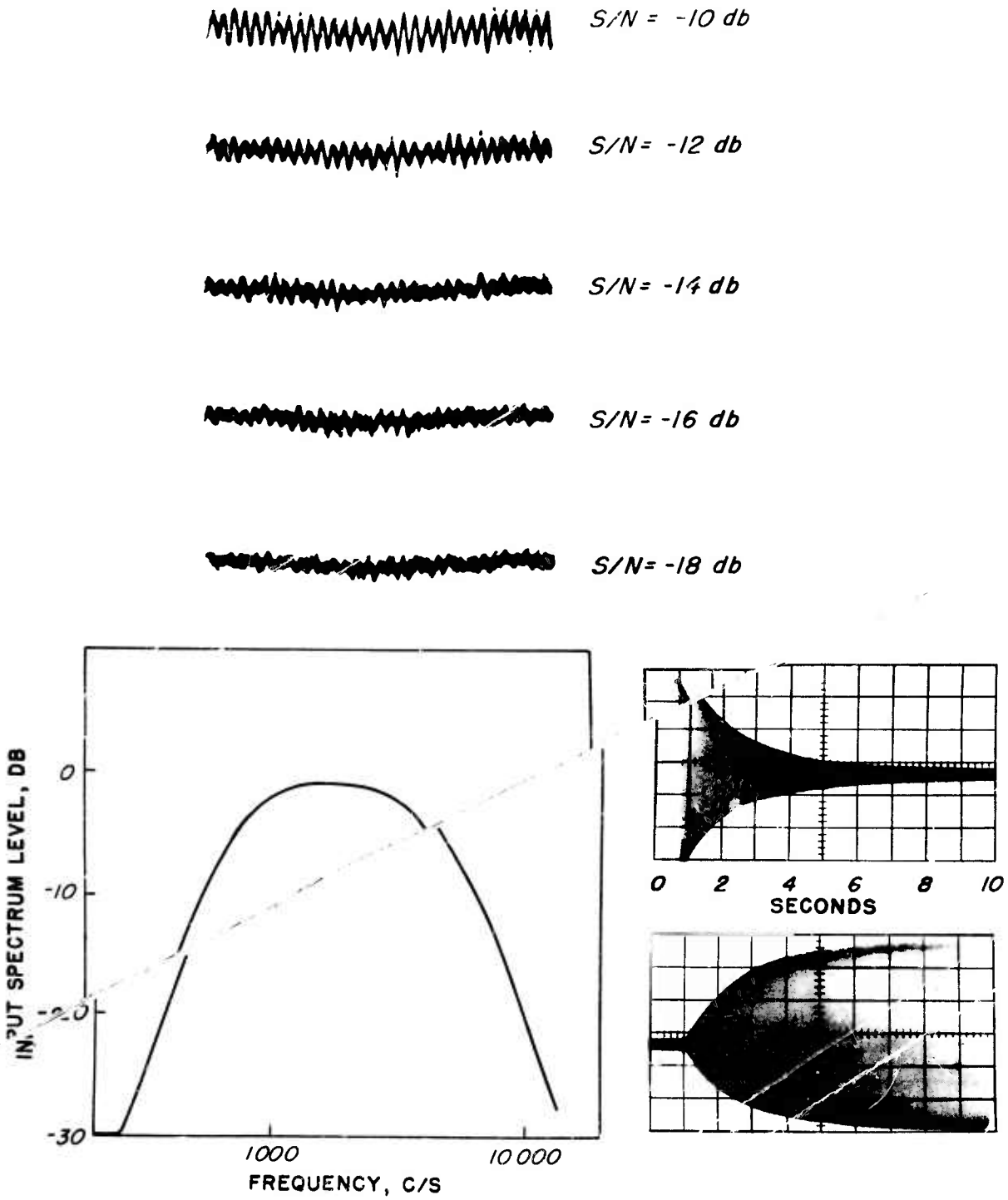

Fig. 40. Deltic correlator output for a number of signal-to-noise ratios near detection threshold. The background noise spectrum and the build-up and decay curves of the dielectric recorder are also shown.

Project X

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